6th ICEE 2022 IEEE

IEEE Advancing Technology for Humanity

6TH IEEE INTERNATIONAL CONFERENCE ON EMERGING ELECTRONICS

11TH-14TH DECEMBER, 2022 | BANGALORE, INDIA

CONFERENCE PROCEEDINGS

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6th IEEE International Conference on Emerging Electronics

6th IEEE ICEE is an in-person conference driven by a vibrant and international technical program committee (TPC) of over 170 industry and academic experts worldwide, enabling a fantastic technical program with a strong industry component. 6th ICEE is expected to hold around 1000 delegates from around the world, with a significant fraction from leading semiconductor industries. The conference includes three plenary addresses & 5 keynote addresses by Industry leaders, over 200 invited speakers with a significant fraction from semiconductor industries, over 250 contributed papers written by around 1000 authors, 170 TPC members, over 20 tutorials & 4 industry sessions offered by industry experts and business leaders. Besides, the conference will host policymakers and attendees from academic institutions and govt. Labs, IT/electronics ministry, semiconductor/VLSI associations in India, and leading semiconductor/VLSI industries. The conference will also host several evening industry sessions, bringing leading industry experts on board to lead debates around pressing topics of industrial importance. Leading semiconductor industries also have signed up for the job fair sessions in the evening. Lastly, ICEE will host sessions such as Women leaders in Semiconductor and young professional mentorship offered by IEEE HQ. ICEE team has built a program/conference which is on par with leading international electron device society's conferences worldwide. We sincerely hope you don't miss this opportunity to learn from each other, network, develop collaborations, and return with some great ideas to work on. We look forward to seeing you at the 6th IEEE ICEE, at Hilton, Manyata Tech park, Bangalore.

Key Highlights of 6th IEEE-ICEE 2022

Technical Symposia

- 3 Plenary Talks
- 5 Keynote Talks
- 200+ Invited Talks
- 120+ Platform/Oral Presentations
- 100+ Poster Presentations
- 1000+ Attendees

Tutorials

5 Tutorial Sessions and Short Courses (6 Hrs) on emerging areas, which are at the verge of shaping the semiconductor technology landscape in the next 5 years

Industry Interaction

Brainstorming sessions to find ways and venues to work closely with Industry. This will a unique platform to build academia – Industry collaboration and draw a 10-year plan/roadmap

Industry Sessions

Heated and seated discussion sessions, in a relaxed setting, on emerging technological areas or key showstoppers or major scientific debates with a quest to find the role academia must play in the next 10 years

Job Fairs

A platform for potential employers to meet their potential hires. ICEE is going to emerge as a one of its kind platforms which ensures that every talent, in the broad field of semiconductor, is seen by potential employers worldwide.

Policy Session and Panel Discussion

To brainstorm the role leading governments must play to put developing economies into the world Semiconductor roadmap

Young Researchers Meet

A special session to explore research opportunities and faculty positions in leading R&D labs and academic institutions in India

Women in Semiconductor

Meet the leading women technologies and scientists and walk through their inspiring journey in the semiconductor world.

Extended Paper in IEEE J-EDS

Top 40 contributed papers will be eligible for an extended paper publication in an special edition of IEEE Journal of Electron Device Society (J-EDS).

Digital & Social Media

Twitter - https://twitter.com/2022Icee
LinkedIn - https://www.linkedin.com/company/79993695/admin/notifications/all/
Facebook - https://www.facebook.com/profile.php?id=100082858363185

Key Dates

July 1st **Call for Papers**	November 5th **Author and Speaker Registration Deadline**
July 15th **Submission Opens**	**November 5th** Technical Program Announcement
September 18th **Submission Closes**	**November 10th** Early Bird Registration Deadline
October 16th **Acceptance of Oral and Poster Papers**	**December 5th** Online Registration Deadline
November 1st **Full Length Paper Submission and Copyright Transfer Deadline**	**December 11th –14th** Conference

Committees

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Department of Electronic Systems Engineering
Indian Institute of Science Bangalore

Technical Program Chair

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Centre for Nano Science and Engineering
Indian Institute of Science Bangalore

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Other Emerging Devices & Computer Technology

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Chemical and Biomolecular Engineering, Vanderbilt University, USA

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Solar Cells & Photodetectors: Physics, Device, & Modules

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Integrated Photonics & Fibre Lasers

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Electrostatic Discharge (ESD) Reliability

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ULSI Circuits/System-on-Chip/Power SoC

Track-Chair
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Energy Storage and Batteries

Track-Chair
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Quantum Device Technologies (QDT)

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Director, IBM Research India & CTO IBM India, and South Asia

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Prof. Umakant Rapol (IISER Pune, India)

Prof. Shouvik Datta (IISER Pune, India)

Prof. R P Singh (Physical Research Laboratory, India)

Theme of IEEE ICEE 2022

IEEE ICEE calls for papers under 22 unique tracks, which broadly fall under (1) Materials, Process & Device Technology, (2) Circuits and Systems and (3) Modeling, Simulation and Reliability.

Materials, Process & Device Technologies

1. Advanced Logic Technologies (ALT)
CMOS platform technologies & opportunities; Logic device performance and circuit design challenges; Advanced, novel process integration schemes and (applications-driven) scaling approaches; Process module innovations and progresses in process control & process metrology; Device technology co-optimization; New or Trending Areas; SiGe channels, GAA (vertically stacked) nanowires and nanosheets based devices and circuits; monolithic 3D integration, 2.5/3D integration; Interconnects (TSV, BEOL, Frontside and Backside connectivity) and BEOL compatible transistors.

2. Advanced Memory Technologies (AMT)
Conventional memories; Emerging memories; 3D memory technologies; Computing-in-memory; New or Trending Areas; Emerging memories for neural networks; Memory-enabled artificial intelligence applications; Memory for bio-inspired computing; System-technology co-optimization; New Memory hierarchy.

3. Neuromorphic Device Technology, Circuits and Systems (NDTCS)
Implementations of neurons, synapses, and other ML/AI circuits employing emerging nanoscale memories, Novel analog and digital CMOS circuits, Novel architectural approaches to implement bio-mimetic computational features, Device-system integration approaches for AI/ML applications.

4. 2D Material Based Technologies (2DT)
Growth related issues, heterostructures, 2D Electronics, 2D Optoelectronics, Sensing Devices, Neuromorphic Devices, 2D Quantum Devices, Other Fundamental engineering, technological and scientific topics related to 2D materials, etc.

5.Other Emerging Devices & Compute Technology (EDCT)
Spintronic and magnetic devices; Steep-slope devices; Topological materials and devices; phase transitions transistors; Emerging state machines; Continuous time dynamical systems; Novel LT/Cryogenic Devices.

6. Quantum Technologies (QT)
Papers are solicited on Superconducting Qubit technologies; Semiconductor Qubits (SiGe, Graphene, etc.); Superconductivity; Single Photon Detectors, Single Photon Emitters; Quantum Photonics, On-chip Photonics; other quantum devices and quantum-enhanced technologies, etc.

7. RF, Millimeter and THz Technologies, Circuits and Systems (RF-THz)
High Performance III-V, III-Nitride and SiGe devices for mm-wave to THz applications; Power device technologies for micro and mm-wave; mm-wave and THz analog front ends, PAs, LNAs and mixers; RF energy harvesting devices and circuits; Packaging of high-frequency devices; Tunable high-Q passives for mmW applications, SAW/BAW devices, device and circuits for 6G applications; onchip antenna arrays and beam forming for mmW and THz applications.

8. Solar cells & photodetectors: Physics, Device, & Modules (SP)
Materials for solar cells, and photodetectors, including Si, III-V, III-N, quantum dots, and hybrid perovskites; Defects; Integration with novel functional substrates; semi-transparent solar cells; tandem solar cells; Functional solar cells like agrivoltaics & building integrated photovoltaics; Photo-physics and advanced characterization; Reliability and packaging of devices; hyperspectral detectors; detectors with unconventional spectral bandwidth, high sensitivity, or high time-resolution; uncooled IR detectors; Topological optoelectronics and photonics; Scale-up; module design and manufacturing; recycling or disposal of solar modules; field studies of solar panels.

9. LED & semiconductor lasers: Device, physics & modules (LL)
Materials for emission including, III-V, III-N, quantum dots, organics semiconductors, and hybrid perovskites; defects and fundamental physics; single-photon emitters; semiconductor lasers; printable LED; large-area LED; high-power LED; multi-band emitters; emitters in unconventional wavelengths like UV and IR; new designs for FPA.

10. Macroelectronics & Displays: devices, circuits & systems (DIS)
Large-area electronics; Flexible electronics; Printable electronics; Wearable electronics; Hybrid organic/inorganic microfabrication and devices; Printing for high-resolution or large-area; Flexible displays; devices and circuits for active and passive display drivers; ultra-high resolution displays; low-power displays; Displays and imagers for augmented or virtual reality; Holographic devices and displays; Displays with unconventional form or size; Imagers with new materials or flexible platform and printed electronics; Intelligent Image Sensors; In-display Sensors; Scale-up.

11. Integrated Photonics & fibre lasers (IPFL)
All types of heterogeneous integrated optoelectronics including sources, modulators or detectors; Optoelectronic integration for neuromorphic computing; SiNx platform; Non-telecom integrated photonics e.g. mid-IR or visible; Fibre lasers and modules with high-power, unconventional wavelengths, or new physics.

12. Sensors and Bio-electronics (SBE)
Sensors includes chemical, molecular and biological detection based on acoustic, electrical, electrochemical, magnetic, mechanical and optical principles; sensors for environmental monitoring e.g. agri-sensors and gas-sensors; sensors for process monitoring; Physical and biochemical integrated sensors; Multi-sensors on a chip for wearable and IoT applications; sensors integrated with energy harvesting; Bio-electronic interfaces and implantable devices; Intelligent sensors with embedded AI; point-of-care biomedical devices; integrated biomedical sensing and implantable neural interfaces; Sensors and devices for human-machine interface; Sensors and motors for haptics.

13. MEMS/NEMS and Heterogeneously Integrated Devices (NEMS)
Micro/nano electromechanical systems (MEMS and NEMS), MEMS for Internet of Things; Microfluidics and BioMEMS (organic-inorganic hybrid devices), CMOS-on-MEMS; MEMs Actuators, resonators and integrated inertial measurement units; TFTs, RF MEMS; micro-optical and optomechanical devices; micro-power generators; MEMs devices for energy harvesting as well as on-chip energy storage.

14. Advanced Power Device Technology (APDT)
High voltage silicon based discrete devices (>200V) such as super junction MOSFETs, IGBTs, thyristors, GTOs and pn-diodes; Low voltage silicon based discrete power devices (≤ 200V) and power devices for power ICs of all voltage ranges; Other power devices, modules and systems; System-level impact of power devices; manufacturing processes, device design, modeling, physics, and reliability of power devices; Fundamental studies on doping, traps, interface states and device reliability for power switching devices; Power device for applications for automotive and aviation to smart grid; Power devices or circuits and its reliability.

15. Wide Bandgap Power Semiconductor Technologies (WPSD)
Wide bandgap and ultra-wide bandgap semiconductors; GaN and compound materials (e.g. AlN, Ga2O3, GaAs) based power devices, technology and integration; materials and processing issues; Lateral heterojunction devices; Vertical GaN transistors and diodes; AlN based power devices; Special circuits and application for GaN and nitride based power devices; GaN and nitride based power IC technology; Reliability physics and failure analysis of GaN basedpower devices; New process integration for GaN power IC; Related simulation or measurement technology; SiC and other material (e.g. Ga2O3, diamond) based power devices, technology and integration; materials and and processing issues, device design, novel device architectures, device reliability, etc.

16. Energy storage and batteries (ESB)
Materials and physics for electrode and electrolytes used in batteries including metal-oxides, nitrides, polymers, hybrid perovskites; advanced characterization; Reliability; photo-rechargeable batteries; batteries for niche application like grid-storage, electric vehicles and IoT; Novel chemistries like flow battery, earth-abundant elements and Na-ion battery; polymer batteries; device-integrated batteries; ultra-capacitors; scale-up and integration challenges.

Circuits and Systems

1. Neuromorphic Device Technology, Circuits and Systems (NDTCS)
Implementations of neurons, synapses, and other ML/AI circuits employing emerging nanoscale memories, Novel analog and digital CMOS circuits, Novel architectural approaches to implement bio-mimetic computational features, Device-system integration approaches for AI/ML applications

2. Quantum Control & Cryogenic Electronics (QCCE)
On chip Control electronics for Quantum Computing; FPGA implementation of Quantum control electronics, Cryogenic RF devices; Cryogenic RF modules, analog and RF front ends, Cryogenic digital processors and controls; Quantum device and Cryogenic electronics integration strategies; thermal management at Cryogenic temperatures; ultra-low power circuit design for on chip Cryogenic quantum control electronics, etc.

3. RF, Millimeter and THz Technologies, Circuits and Systems (RF-THz)
High Performance III-V, III-Nitride and SiGe devices for mm-wave to THz applications; Power device technologies for micro and mm-wave; mm-wave and THz analog front ends, PAs, LNAs and mixers; RF energy harvesting devices and circuits; Packaging of high-frequency devices; Tunable high-Q passives for mmW applications, SAW/BAW devices, device and circuits for 6G applications; onchip antenna arrays and beam forming for mmW and THz applications.

4. Advanced Power Device Technology (APDT)
High voltage silicon based discrete devices (>200V) such as super junction MOSFETs, IGBTs, thyristors, GTOs and pn-diodes; Low voltage silicon based discrete power devices (≤ 200V) and power devices for power ICs of all voltage ranges; Other power devices, modules and systems; System-level impact of power devices; manufacturing processes, device design, modeling, physics, and reliability of power devices; Fundamental studies on doping, traps, interface states and device reliability for power switching devices; Power device for applications for automotive and aviation to smart grid; Power devices or circuits and its reliability.

5. Wide Bandgap Device Based Circuits and Systems (WDCS)
Power electronic systems based on Wide bandgap devices, system level reliability issues in WBG power electronic systems; Gate driver IC design including WBG power device applications; Circuit design for SiC and GaN based IC; New circuit and layout design enhancing power IC performance; Single chip inverters and converters; New signal isolation technology on power IC such as magnetic coupling.

6. ULSI Circuits/System-on-Chip/Power SoC (SoC)
Analog and mixed signal design in advanced nodes; High speed interfaces; mmW Circuits in Si technology nodes; Radar on Chip; AI accelerators, edge computing, on-chip power management circuits; automotive chip modules; ultra-low power and low noise circuits; on-chip RF amplifiers for 5G applications; SoC challenges in sub-7nm CMOS nodes; RF design challenges in sub-7nm nodes; high-voltage design challenges in sub-7nm nodes; new chip architectures; chip package co-design; Power IC, Power SoC, and Automotive Chip modules, etc.

Modeling, Simulation & Reliability

1. Reliability Physics of Semiconductor Devices (RPSD)
Reliability of FEOL/MEOL/BEOL, Design for reliability and variability-aware design, variability in advance and emerging device technologies; Robustness and security of electronic circuits and systems; Reliability of devices and systems for biomedical, automotive and aerospace; Reliable systems with unreliable devices; Reliability of cryogenic devices for future quantum computing applications; Noise characterization; Degradation mechanisms of emerging memories; Reliability of devices, circuits and systems for more-than-Moore; Reliability of biomedical devices, circuits and systems; Reliability of automotive and aerospace devices circuits and systems.

2. Electrostatic Discharge Reliability (ESD)
ESD reliability in advanced CMOS and beyond CMOS technology nodes, ESD behaviour of emerging technologies; ESD device physics; latch-up issues in advanced CMOS nodes; ESD issues and protection methodology in GaN based circuits/systems; ESD behaviour and physics in 2D materials; ESD device modelling approaches; Full chip verification methodology; System level ESD and SEED.

3. Modelling and Simulations (MS)
Technology CAD and benchmarking for novel/emerging technologies; atomistic process and device simulations; Compact models for emerging/novel devices (supported by experiments); Modelling of alternative computing devices; material and interconnect modeling; advanced packaging and 3D integration modeling; device modeling for photonic, quantum, neuromorphic devices; modeling of power and RF devices; fundamental and physical insights into fundamental processes or technological showstoppers in different device types, etc.

Program Overview

Day 0 (Sunday, Dec 11th)

09:30 AM - 01:00 PM : Tutorials [Audi 4 – 8]
01:00 PM - 02:30 PM : Lunch (Terrace)
02:30 PM - 06:00 PM : Tutorials [Audi 4 – 8]
06:00 PM - 09:00 PM : Upload your slides for Day 1 (Speaker Room)

Day 1 (Monday, Dec 12th)

07:00 AM - 08:45 AM : Breakfast [Terrace] & Upload Your Slides for Day 1 [Speaker Room]
09:00 AM - 09:10 AM : Inauguration [Audi 1-3]
09:10 AM - 09:20 AM : EDS President Inaugural Note [Audi 1-3]
09:20 AM - 09:25 AM : EDS VP for Education [Audi 1-3]
09:25 AM - 10:30 AM : Plenary 1 - Dr. Alessandro Curioni (IBM) [Audi 1-3]
10:30 AM - 11:15 AM : Industry Keynote 1 - Dr. Julio Costa (Global Foundries) [Audi 1-3]
11:15 AM - 11:30 AM : Session Break - Grab Your Quick Tea
11:30 AM - 12:15 PM : Industry Keynote 2 - Dr. Carlos Castro (Nexperia) [Audi 1-3]
12:15 PM - 01:00 PM : Industry Keynote 3 - Mr. Anand Ramamoorthy (Micron) [Audi 1-3]
01:00 PM - 02:30 PM : Lunch & Networking (Terrace)
02:30 PM - 04:15 PM : 11 Parallel Sessions [Audi 1-11]
04:15 PM - 04:30 PM : Session Break - Grab Your Quick Coffee
04:30 PM - 06:00 PM : 11 Parallel Sessions [Audi 1-11]
06:30 PM - 08:00 PM : Job Fair/Talk Over Starters [Audi 11]
06:30 PM - 08:00 PM : WiSEMI & YRM [Over Starters] [Audi 8]
06:30 PM - 08:00 PM : Evening Industry Sessions 1 & 2 [Over Starters] [Audi: 1 & 2]
07:00 PM - 09:00 PM : Poster Session – 1 [Over Starters] [Audi: 3]
08:30 PM - 10:00 PM : Dinner - General Chair's Reception (Terrace)
06:30 PM - 08:30 PM : Upload your slides for Day 2 [Speaker Room]

Day 2 (Tuesday, Dec 13th)

07:00 AM - 08:45 AM : Breakfast (Terrace)
09:00 AM - 10:00 AM : Plenary 2 - Mr. Sameer Pendharkar (TI) [Audi 1-3]
10:00 AM - 10:45 AM : Industry Keynote 4 - Dr. Primit Parekh (Transphorm) [Audi 1-3]
10:45 AM - 11:15 AM : Tea, Coffee & Networking
11:15 AM - 01:00 PM : 11 Parallel Sessions [Audi 1-11]
01:00 PM - 02:30 PM : Lunch & Networking (Terrace)
02:30 PM - 04:15 PM : 11 Parallel Sessions [Audi 1-11]
04:15 PM - 04:30 PM : Session Break - Grab Your Quick Coffee
04:30 PM - 06:00 PM : 11 Parallel Sessions [Audi 1-11]
06:30 PM - 08:00 PM : Job Fair/Talk [Over Starters] [Audi 1-11]
06:30 PM - 08:00 PM : Evening Industry Sessions 3 & 4 [Over Starters] [Audi: 1 & 2]
07:00 PM - 09:00 PM : Poster Session - 2 [Over Starters] [Audi: 3]
08:30 PM - 10:00 PM : Conference Dinner (Terrace)
06:00 PM - 08:30 PM : Upload your slides for Day 3 [Speaker Room]

Day 3 (Wednesday, Dec 14th)

07:00 AM - 08:45 AM : Breakfast (Terrace)
09:00 AM - 10:00 AM : Plenary 3 - Mr. Balajee Sowrirajan (Samsung) [Audi 1-3]
10:00 AM - 10:45 AM : Industry Keynote 5 - Dr. Milind Kulkarni (Reliance) [Audi 1-3]
10:45 AM - 11:15 AM : Tea, Coffee & Networking
11:15 AM - 01:00 PM : 11 Parallel Sessions [Audi 1-11]
01:00 PM - 02:30 PM : Lunch & Networking (Terrace)
02:30 PM - 04:15 PM : 11 Parallel Sessions [Audi 1-11]
04:15 PM - 04:30 PM : Session Break - Grab Your Quick Coffee
04:30 PM - 06:30 PM : IEEE EDS Young Professional (YP) [Audi: 11]
04:30 PM - 06:30 PM : 11 Parallel Sessions [Audi 1-11]
07:00 PM - 08:00 PM : Closing Ceremony & Awards [Audi 1-3]
08:00 PM - 10:00 PM : Thanksgiving Dinner (Terrace)

Industry and Plenary Keynote Talk

Plenary 1: IBM's Quantum and Future of Computing
Dec 12th, 2022, Grand Ballroom, 9:30 AM - 10:30 AM
Speaker: Dr. Alessandro Curioni (IBM Fellow, Vice President, IBM, Europe & Africa and Director, IBM Research, Zurich, Switzerland)
Session Chair: Prof. V. Ramgopal Rao (IEEE Fellow, Pillay Chair Professor & Past Director, IIT Delhi)

Abstract: Computing is poised to reshape just about every industry, field of study — and even society itself. Across the fields of AI, cloud, and quantum computing, we've seen substantial advancements. The most profound advancements will be reached, though, by the convergence of classical computing, artificial intelligence and quantum, through the cloud. The result will be enormous computational power poised to fundamentally change the way we innovate and discover. In my presentation, I will discuss the latest trends, the open questions and how the academic and industrial communities may synergize to accelerate the rate of scientific discovery.

Plenary 2: Analog and Power Technologies for Industrial and Automotive Electronics
Dec 13th, 2022, Grand Ballroom, 9:00 AM - 10:00 AM
Speaker: Mr. Sameer Pendharkar (Vice President, Technology Development and TI Senior Fellow at Texas Instruments)
Session Chair: Dr. Ravi Todi, Sr. Technologist, Western Digital Inc, USA

Abstract: With increase in per capita energy consumption and limited energy resources, it is critical to not only look at alternate energy sources but also to improve the efficiency in how this energy is used. New advances in semiconductor materials and technologies continue driving increasing electronics adoption in industrial and automotive systems making them more efficient. Innovations in multi-domain mixed signal integration are driving Industry 4.0 whereas significant improvements in power density and high voltage technology are enabling automotive electrification. The talk will focus on the trends and performance improvements in both the silicon and WBG semiconductor IC technologies targeted for these applications and also discuss the manufacturing challenges and opportunities for these technologies.

Plenary 3: System Solutions Powering Intelligent Connected Device
Dec 14th, 2022, Grand Ballroom, 9:00 AM - 10:00 AM
Speaker: Mr. Balajee Sowrirajan (Vice President, Samsung Electronics & MD Samsung Semiconductor R&D, India)
Session Chair: Prof. Rudra Pratap, Founding Vice Chancellor, Plaksha University, India

Abstract: With Industrial Revolution 4.0 driving exciting use models, system solutions are powered by devices which are not just connected, but also Intelligent. The talk will focus on fundamental technology anchors – Connectivity, Sensors, Big Data and AI Processing solutions. It will focus on the technological advancements in these areas which are and will be transforming our day to day lives.

Keynote 1: RFSOI Technology for the RF Front-End: Then, Now and Tomorrow
Dec 12th, 2022, Grand Ballroom, 10:30 AM - 11:15 AM
Speaker: Dr. Julio Costa (VP RF, Technology and Innovation, Global Foundries, Santa Clara CA, USA)
Session Chair: Prof. V. Ramgopal Rao (IEEE Fellow, Pillay Chair Professor & Past Director, IIT Delhi)

Abstract: RFSOI technologies are used today in the RF section of all cellular handsets, performing a number of different critical RF switching and tuning functions, and recently also providing an even larger number of low noise amplifiers, digital CMOS blocks and critical analog functions. This talk will discuss the history of RFSOI technology, the critical enablers that allowed it to in a relatively short amount of time, completely replace the existing III-V switch technologies. The progression to today's modern RFSOI technologies and its array of device options will also be described, as well as future trends in RF switching technologies. In particular, the RF front end of the future will incorporate a number of 3D technologies in both die-to-wafer and wafer-to-wafer bonding approaches in order to reduce critical dimensions while providing superior RF performance.

Keynote 2: Power Semiconductor Technologies: a future pure WBG game?
Dec 12th, 2022, Grand Ballroom, 11:30 AM - 12:15 PM
Speaker: Dr. Carlos Castro (Vice President & General Manager Nexperia, Germany)
Session Chair: Prof. Subramanian Iyer, Distinguished Chancellor's Professor, University of California, USA

Abstract: The current power semiconductor market is still largely dominated by silicon-based devices. However, SiC penetration is growing very fast for new generation of systems and applications to come. Furthermore, with GaN offering significant benefits for increasing efficiency, power density and reducing cost, the question is if all three technologies will complement or replace each other. This presentation will reflect driving elements at different applications influencing the selection of technologies.

Keynote 3: Memory at the Heart of Intelligence
Dec 12th, 2022, Grand Ballroom, 12:15 PM - 1:00 PM
Speaker: Mr. Anand Ramamoorthy (Managing Director & Vice President, Micron, India)
Session Chair: Prof. Subramanian Iyer, Distinguished Chancellor's Professor, University of California, USA

Abstract: As technology continues to be the key enabler of human development, data is at the heart of the new dynamics that is shaping our world.At the heart of this reimagined world is data, creating opportunity for new computing use cases and demanding new hardware foundations to feed applications faster and more efficiently. Memory and storage innovation drives that data hardware foundation that will unleash broadscale AI adoption, reshape data center computing, accelerate intelligent edge proliferation, and enable user experiences not yet imagined.The memory hierarchy is seeing a significant evolution where trends such as very large AI systems, 5G and data movement, autonomous driving and edge intelligence amongst others, are fueling the need for refined and customized memory solutions – both for the DRAM as well as the storage applications. We are also seeing changes in the compute paradigms to recognize this evolving data centric model, leading to the emergence of new protocols. All these together pose a complex set of challenges to memory solutions across the board in terms of technology, materials, packaging and systems. In this talk, we will dwell on these trends and we will talk about some of the exciting opportunities that are in front of us to enable the next generations of memory.

Keynote 4: Manufacturing and Commercialization of Easy to Use, Robust, High Performance GaN Power Devices – from 650V to 1200V, from 45W to 10kW+
Dec 13th, 2022, Grand Ballroom, 10:00 AM - 10:45 AM
Speaker: Dr. Primit Parekh (Co-Founder & President, Transphorm Inc., USA)
Session Chair: Dr. Ravi Todi, Sr. Technologist, Western Digital Inc, USA

Abstract: GaN technology needs to serve the broadest market to be a viable solution in the long term. Transphorm's robust normally-off GaN FET with its integrated Si-GaN architecture provides easy to interface, highest performance solutions with the best in class proven reliability with over 80 billion hours in the field: from low wattage markets such as adapters/chargers through Titanium-class power supplies to Renewable Energy to Electric Vehicles solutions such as on-board chargers and DC/DC converters today and traction tomorrow. With its vertically integrated wafer manufacturing providing control, scale and rapid innovation backed by one of the strongest IP portfolio in GaN power, Transphorm provides the GaN industry's first 650V and 900V AEC-Q101 product with 1200V in its roadmap. This presentation will detail how Transphorm's GaN solutions enable our customers to serve the broadest and fastest growing power conversion markets – from low power to high power, from adapters to automotive as well as GaN manufacturing, including in the context of India's Semiconductor Mission.

Keynote 5: Solar Value Chain: Historical Evolution, Technology platforms, and Roadmap
Dec 12th, 2022, Grand Ballroom, 10:00 AM - 10:45 AM
Speaker: Dr. Milind Kulkarni (President, PV Manufacturing, Reliance Industries, India)
Session Chair: Prof. Rudra Pratap, Founding Vice Chancellor, Plaksha University, India

Abstract: Solar energy has become commercially attractive on the foundation of semiconductor polysilicon, crystal, and wafer processing technologies, complemented by the emergence of efficient cell technologies founded on unit operations well-established in the semiconductor industry. These technology platforms will further push product performance and can deliver module cash cost less than $0.12/W and LCOE less and $0.02/kWh (DC) over the next 5-year horizon. In addition, more attractive new technology platforms are emerging. This talk focuses on both technical and commercial aspects of the solar value chain and opportunities ahead.

Tutorials (Sunday, Dec 11th)

Tutorial – I: A Journey from sub-6 GHz to Tera Hz - Applications, Design, Circuits, and Technologies
Chair: Dr. Anirban Bandyopadhyay, GlobalFoundries, USA | Audi: 4

Learning Outcomes: In this tutorial, we'll talk about the fundamentals of RF, mmWave and THz (>100GHz) radio covering different application and system requirements, circuits and design aspects and technologies. We'll also highlight the key challenges to the radio system performance as we go to higher frequencies and how state-of-the -art technologies can address those challenges with innovations in materials, circuits, and system levels. The attendees will hear from some of the experts in this area how the future mmWave and Sub THz radio will look like and where current research is focused on at both industry and academic institutions for communication, sensing and spectroscopy.

Instructors:
1. Ned Cahoon, GF, USA
2. Vadim Issakov, Universty of Braunschweig
3. Venkata Vanukuru, GF
4. Eric Desbonnets, SOITEC
5. Dibakar Roychowdhury, Mahindra University

Session 1: Overview of challenges and trends in Wireless applications (Dr. Ned Cahoon) – 1.5 Hrs

Key Topics covered
- Key challenges of a cellular radio link
- Why are higher frequencies like mmWave (24-100GHz) and sub-THz (>100GHz) needed
- Key challenges of mmWave and sub-THz Radio
- Different Phased array systems and beamforming techniques

Key learning goal:
Fundamentals of mm-wave Sub-THz radio, basics of phased array antenna and how it helps.

Session 2: Design basics and challenges for RF, mmWave & THz (Dr. Vadim Issakov) – 1.5 Hrs.
Key Topics covered
- Different Analog vs. RF vs. mm-Wave Design Approaches
- Fundamental Concepts of matching à to match or not to match
- Passive Components on-chip (TLine, Inductor, Transformer, Varactor)
- Design Basics and Challenges for Key blocks (LNA, PA, VCO)

Key learning goal:
Basic design methodologies for mm-wave and Sub-THz radio components

Session 3: Key RF and mm-wave circuits blocks - state of the art and innovations (Dr. Venkat Vanukuru) – 1.5 Hrs

Key Topics covered
- Switch, LNA and PA integration on SOI/SiGe technologies
- Challenges and opportunities for RF and mmWave.
- Circuit innovations, technology features, KPI's
- State of the art performance numbers for all the above circuit blocks.

Key learning goal:
Technology dependence of mm-Wave Switch, LNA PA performance, key challenges and innovative circuit techniques to address those.

Session 4: Semiconductor Technologies and materials to address RF, mm-wave, THz communications, sensing and spectroscopy (Dr. Eric Desbonnets, and Dr. Dibakar Roychowdhury) – 1.5 Hrs

Key topics covered:
- RF and mmWave Radio systems specifications for 5G advanced and future 6G requirements
- Comparison between bulk silicon, SOI, SiGe and non-silicon materials for 5G advanced and future 6G.
- Different THz sensing and spectroscopic techniques, pros and cons, trend

Key learning goal:
Comparison among different Si and non-Si technologies for mm Wave 5G and sub-THz 6G; how sensing works at THz frequencies, familiarity with different THz spectroscopic techniques and applications.

Tutorial – II: Industry Standard Compact Models for Advanced Semiconductor Devices
Chair: Prof. Yogesh Chauhan, IIT Kanpur, India | Audi: 5

Learning Outcomes:

- Understanding of semiconductor device concepts
- Compact modelling techniques
- Implementation of compact model in circuit simulator

Instructors:

1. Nihar Ranjan Mohapatra, IIT Gandhinagar, Gandhinagar
2. Anjan Chakravorty, IIT Madras, Chennai
3. Avirup Dasgupta, IIT Roorkee, Roorkee
4. Somu Ghosh, Texas Instruments, Bengaluru

Session 1: Introduction to Compact Modelling (Dr. Avirup Dasgupta and Dr. Nihar Ranjan Mohapatra) – 0.5 Hrs

Key Topics Covered:
The compact model represents the behaviour of semiconductor devices in form of equations. The compact models play an important role in designing integrated circuits and serves as a bridge to share the information between foundries and circuit designers. Since various flavours of semiconductor devices have been proposed for a myriad of applications, the compact models have also evolved in last few decades. Accurate, fast, and robust compact models, which are capable of reproducing very complicated device characteristics are need of the hour.

Key learning goal:
Introduction to the compact model and art of compact modelling.

Session 2: BSIM – An Industry Standard Compact Model for FinFETs and beyond (Dr. Avirup Dasgupta) – 1.5 Hrs.

Key Topics Covered:
The MOS transistor architecture has evolved in last few decades. The semiconductor industry has progressed from bulk MOSFETs to FinFETs in 22nm CMOS technology and nanosheet FETs in 3nm CMOS technology. The device physics and device characteristics have also become complex.

This part of the tutorial will describe the BSIM family of industry-standard compact models for modern and future devices at advanced technology nodes. The discussion will range all the way from core models to the more involved second-order effects like quantum confinement, short-channel effects, noise etc.

Key learning goal:
Inner workings of the latest BSIM model framework and how it captures the characteristics of advanced devices efficiently.

Session 3: HISIM-HV – An Industry Standard Compact Model for High Voltage and High-Power Devices (Dr. Nihar Ranjan Mohapatra) – 1.5 Hrs

Key Topics Covered:
The use of high-voltage and high-power MOS devices like Drain Extended MOS (DEMOS) transistors and Laterally Diffused MOS (LDMOS) transistors have been increasing since last two decades. The applications like automotive electronics, mobile communication, power conversion/conditioning in smart grids with renewable energy sources will not be possible without use of these devices. The device architecture, device characteristics and figures of merit of high voltage devices are completely different from the conventional MOS structures. The phenomena like on-state breakdown, off-state breakdown, quasi saturation, KIRK effect are unique to these devices.

Key learning goal:
HISIM-HV industry-standard compact model for silicon based high voltage devices. The discussion will range all the way from core model to the advanced models emulating different anomalous device behavior (like capacitance, internal drain voltage) of HV devices.

Session 4: HICUM – An Industry Standard Compact Model for Homo and Heterojunction Bipolar Transistors (Dr. Anjan Chakravorty) – 1.5 Hrs

Key Topics Covered:
The Heterojunction Bipolar Transistor (HBT), an advanced version of Bipolar Junction Transistor (BJT), has been widely used in modern ultrafast circuits and in applications requiring high power efficiency (such as power amplifiers in communication systems). The HBTs have shown lots of promise for terahertz applications such as high-speed communications, spectroscopy and imaging. The bipolar devices are completely different from the MOS devices.This part of the tutorial will discuss the HICUM industry-standard compact models for HBTs. The discussion will start with a typical diode model implementation in Verilog-A followed by, (a) the introduction of the integral charge control relation (ICCR) based SPICE Gummel-Poon model for bipolar junction transistor and (b) modern heterojunction bipolar transistor model, HICUM.

Key learning goal:
1. 1-D intrinsic and 2-D internal HICUM model equivalent circuits, element formulations and corresponding parameter extraction strategies. 2. Recent improvements from perspectives of non-quasistatic delay, noise correlation and self-heating effects.

Session 5: Introduction to Process Design Kit (PDK) Development (Mr. Somu Ghosh) – 1.0 Hr.

Key Topics Covered:
The compact models, after development, are included in the Process Design Kit (PDK). Along with the compact model, the PDK generally consists of files such as device library, design verification decks and design rule manual. The PDKs are released by the technology companies to the designers for circuit and system design with different technology nodes. In an enterprise environment, the designers consume and build on technology information using the PDK.

Key learning goal:
PDK development flow, consumables that go into the PDK and philosophy and design practices that are associated with building the PDK. This tutorial will provide an umbrella view of the PDK and unique aspects of building PDK for different CMOS technologies.

Tutorial – III: Neuromorphic Computing
Chair: Prof. Bipin Rajendran, King's College London, UK | Audi: 6

Learning Outcomes: To develop theoretical understanding on machine learning and neural networks. To understand requirements for its hardware implementation, and how to do digital, analog, and mixed-signal implementations of neuromorphic hardware.

Instructors:
1. Chandramani Singh, IISc, Bangalore
2. Debanjan Bhowmik, IIT Bombay
3. Shubham Sahay, IIT Kanpur
4. Sandip Mondal, IIT Bombay

Session 1: A brief introduction to a few Machine Learning Techniques (Prof. Chandramani Singh) – 1.0 Hr.

Key Topics Covered:
The focus of this tutorial will be on the theoretical underpinnings of machine learning. We will start with a brief introduction of the machine leaning paradigms, i.e., supervised, unsupervised and reinforcement learnings. We will then have an overview of several learning techniques, e.g., linear regression, logistic regression, neural networks, backpropagation, K-means etc. We will touch upon the underlying mathematical tools like gradient descent, kernels, singular value decomposition etc. Finally, we will discuss complexities and performance measures of the above techniques and a few illustrative applications.

Key learning goal: Machine learning techniques

Session 2: Neuromorphic Computing: Basics, Requirements for hardware implementation, and Applications (Prof. Debanjan Bhowmik) – 1.0 Hr.

Key Topics Covered:
Neuromorphic computing will be introduced here both from a biology perspective and a computer-science/ machine-learning (ML) perspective. Importance of coming up with new hardware to implement the algorithms will be explained. As emerging hardware platforms, both analog/ mixed-signal hardware and digital hardware will be briefly introduced. Potential applications like edge artificial intelligence and robotics will also be covered.

Key learning goal: 1. Varied applications of Neuromorphic computing. 2. Hardware platforms for Neuromorphic computing

Session 3: Digital (CMOS) and Mixed-Signal Implementations and Hardware: From architecture to demonstrated implementations (Prof. Shubham Sahay) – 1.0 Hr.

Key Topics Covered:
Digital and mixed-signal hardware for neuromorphic computing will be covered in details in this talk. Crossbar arrays of non-volatile memory (NVM) synaptic devices will be introduced in the context of mixed-signal hardware, with a discussion on how to perform multiply-accumulate (MAC) and Vector-by-Matrix Multiplication (VMM) operations on these arrays and the requirements from the synaptic devices for the purpose.

Key learning goal: Digital and mixed-signal hardware

Session 4: Neuromorphic Hardware: Analog Implementations / RRAM (and related memory device) based implementations (Prof. Sandip Mondal) – 1.0 Hr.

Key Topics Covered:
The physics of operation of resistive random-access memory (RRAM) devices will be covered here. It will be explained how such physics can be utilized to obtain biologically inspired synaptic behaviour in RRAM devices and make them suitable for analog and mixed-signal hardware applications, discussed in the previous talks.

Key learning goal: Physics of RRAM devices

Tutorial – IV: Biosensors and Flexible Electronics
Chairs: Prof. Siddhartha Panda, IIT Kanpur, India & Prof. Shree Prakash Tiwari, IIT Jodhpur, India | Audi: 7

Learning Outcomes:
- Flexible bioelectronics on thread or textile substrate.
- To develop flexible bioelectronics for precision medicine using threads/textiles as substrate.
- Translation of biosensors towards products.
- Considerations for bringing a product into market
- Flexible Electronics: Challenges, Perspectives and Limitations for a rapidly expanding technology

Instructors:
1. Sameer Sonkusale, Tufts University, USA
2. Chandrasekhar Nair, Bigtec Labs, Bengaluru, India
3. S. Sundar Kumar Iyer, IIT Kanpur, India
4. Canterella Guiseppe, Free University of Bozen-Bolzano, Italy

Session 1: Flexible bioelectronics on thread or textile substrate (Prof. Sameer Sonkusale) – 1.5 Hrs

Key Topics Covered:
This tutorial will explore the new realm of using threads and textile as an ultimate platform for flexible and stretchable bioelectronics. Threads offer unique advantages of universal availability, low cost, material diversity and simple textile-based processing. Interestingly, threads also provide an ideal platform for passive microfluidic sampling and delivery of analytes. In this talk, I will report reel-to-reel fabrication of functional smart threads for variety of sensing and electronics application. I will report on nanomaterial-infused smart threads for sensing strain and temperature. Nano-infused threads will be presented for sensing pH, glucose, lactate, ammonium and other chemical and biological biomarkers directly in biological fluids such as sweat or wound exudate. Beyond sensing

and microfluidics, I will present recent progress on making super-thin transistors and electronics directly on thread and textile substrates. This new toolkit of highly flexible thread-based microfluidics, sensors, transistors and electronics makes it possible to realize wearable and implantable sensor platforms for health monitoring and treatment. The tutorial will showcase multiple applications for thread-based flexible biolectronics, such as wearable sweat sensing patches for monitoring metabolic health, smart bandages for treatment of chronic wounds, and smart sutures for detection and treatment of surgical infections. Tutorial will provide a roadmap for this emerging field and relevance to the ICEE scientific community.

Key learning goal: To develop flexible bioelectronics for precision medicine using threads/textiles as substrate.
Session 2: Biosensors: Challenges in translating concepts to products (Dr. Chandrasekhar Nair) – 1.5 Hrs.

Key Topics Covered:
This talk will cover the various challenges in translating a concept of a biosensor to a product in the market deployed at scale and the strategies to mitigate the risk of failure along the path of translation. The talk will draw heavily on the experiences in scaling Truenat as a Point of care platform for Infectious Disease Detection. The topics covered will include Target Product Profile definitions, market research and inputs, regulatory framework & guidelines (FDA/ CLSI/ WHO PQ), Initial research; from screening concepts to functional prototypes – criteria to be used, identification of critical technology element(s), Intellectual Property Rights: Defensive and Offensive ways, Product development eco-system – the gaps, TRL & MRL levels, FMEA and Technology transfer.

Key learning goal: Translation of biosensors towards products. Considerations for bringing a product into market.

Session 3: Flexible Electronics – an introductory overview (Prof. S. Sundar Kumar Iyer) – 1.5 Hrs.

Key Topics Covered:
The tutorial will start with an introduction and motivation for the emerging area of flexible electronics. The aspects this technology that makes it distinct from conventional electronics and its current limitations would be highlighted. The broad domains of active research and innovations in the area would then be discussed. The tutorial would conclude with some examples of successful and potential future implementation of the technology in real-world products and applications.

Key learning goal: An appreciation for the possibilities and limitations of the area of flexible electronics along with potential domains of research and innovation in that area.

Session 4: Flexible Electronics: Challenges, Perspectives and Limitations for a rapidly expanding technology (Dr. Canterella Guiseppe) – 1.5 Hrs.

Key Topics Covered:
This tutorial will guide the audience through a journey in the field of flexible electronics. Here, a broad plethora of sensors, circuits and systems, capable to withstand mechanical strain (i.e. bending, twisting, stretching, etc..), will be presented. First, an introduction and motivation will be given. Afterwards, the state-of-the-art will be presented, to provide a comprehensive overview in industrial and academic research. Next, materials, fabrication methods and devices will be presented, with a special focus on as stretchable, transparent and green electronics. Systems and real-application scenarios will be also explored. Finally, outlook and challenges for future market growth will be analysed.

Pre-Requisite: Basic knowledge of semiconductor physics and electronic devices.

Key learning goal: Comprehensive overview of a fast-growing technology, based on alternative fabrication strategies and materials.

Tutorial – V: Photovoltaics
Chair: Prof. Anil Kottantharayil, Professor, IIT Bombay, India | Audi: 8

Learning Outcomes:
- Recent advances in organic materials for solar cells.
- Design rules and characterization for new materials for advanced devices. Advances in next-generation singlet-fission chromophores.
- Advanced characterization of commercial silicon solar cells.
- Photovoltaic Module Design and Reliability.

Instructors:

1. Satish Patil, Indian Institute of Science, Bengaluru
2. KL Narasimhan, Indian Institute of Science, Bengaluru
3. Dinesh Kabra, Indian Institute of Technology Bombay, Mumbai
4. Narendra Shiradkar, Indian Institute of Technology Bombay, Mumbai

Session 1: Recent advances in organic materials for solar cells (Prof. Satish Patil) – 1.5 Hrs

Key Topics Covered:
The focus of this tutorial is novel materials. Primarily we shall discuss the class of organic materials used in most thin-film solar cell technologies. In organic photovoltaics, light absorption mostly happens in donor/acceptor heterojunctions. Recent advances in non-fullerene acceptors (NFA) have enabled more than 18% efficiency. Organic materials are also used as hole and electron transport layers. The performance of thin-film solar cells is often limited by the quality and stability of the perovskite/organic interface. Finally, organic chromophores undergo singlet-fission, which can increase the power conversion efficiency beyond the Shockley-Queisser limit. The tutorial will discuss the latest trends in NFAs, transport layers, and S-G chromophores. We shall explore the challenges and opportunities. We shall also discuss the essential characterization techniques.

Key learning goal: Design rules and characterization for new materials for advanced devices. Advances in next-generation singlet-fission chromophores.

Session 2: How to design efficient organic and perovskite thin-film solar cells (Prof. Dinesh Kabra) – 1.5 Hrs.

Key Topics Covered:
The focus of this tutorial is the device physics of thin-film solar cells. Attendees will take a journey, from materials to devices, with solution-processable thin-film organic and perovskite photovoltaics. We will start with a primer on how to choose suitable materials. We shall discuss techniques to evaluate materials based on their photophysics. Specifically, we learn how to screen materials with advanced spectroscopic methods. Given the material properties, we shall learn how to fabricate and characterize thin-film photovoltaic devices. Finally, we shall appreciate the importance of material and device engineering to ensure that the lab-scale device can be upscaled and commercialized.

Key learning goal: How to select materials and design efficient devices for next-generation thin-film solar cells

Session 3: Advanced characterization of commercial silicon solar cells (Prof. K L Narasimhan) – 1.5 Hrs

Key Topics Covered:
This tutorial will focus on solar cell characterization with an emphasis on crystalline solar cells. The tutorial begins with a brief introduction to the basics of solar cells. This is followed by different methods to characterize solar cells- like quantum efficiency, photoluminescence imaging, implied Voc, PFF etc. The tutorial will conclude with a brief discussion of the limitations of the Al-BSF architecture and how advanced architectures like PERC, TOPCON and HJT improve performance.

Key learning goal: Defect analysis and troubleshooting of silicon solar cells.

Session 4: Photovoltaic Module Design and Reliability (Prof. Narendra Shiradkar) – 1.5 Hrs

Key Topics Covered:
Eventual goal of any solar cell technology is to deliver desired performance for several decades in often harsh end-use environments. This is a crucial factor in the commercial success of any PV technology. In this tutorial, we will discuss the design of Photovoltaic modules, materials, and components. We will also look at key performance metrics for PV modules and reliability issues found in the field. Eventually, we will discuss the ways to design high-quality, reliable PV modules.

Key learning goal: Designing of reliable Photovoltaic modules and their performance metrics

Industry Session

Evening Industry Session at 6th IEEE ICEE:
This a special session, which is driven/lead by a senior (Senior Fellow, CXX or equivalent) industry professional and 4-5 other senior panellists from Industry. These will drive the session on a pressing topic of industrial importance while touching a wider audience. We will have 5-6 evening industry sessions (on day 1 & 2), each expected to host around 300+ people, including other business leaders and policy makers / people from the govt. Several business leaders and policy makers will be invited for this session. The industry session is expected to open up discussion on a pressing matter of industrial importance on which role of govt., academia and industry are equally important. It can also be any other pressing topic which requires attention.

Format:
After the chair opens the thread (she/he may use slides), other panellists may add to it. Subsequent to this the session will be open for an open discussion. The session is expected to

1. Develop a better synergy between industry – academia – govt. on the topic under discussion,
2. Develop pointers for govt. to take into consideration when it comes to policy making and
3. Develop pointers for academicians to take up challenging threads in future.

A session may also results in a white paper, which will be circulated across attendees, business leaders and policy makers.

Sessions & Panel Details:

Industry Session – I: How India Can Become a World Leader in Semiconductors by Delivering its Own IP Differentiated Value in Multiple Dimensions of this Industry
Dec 12th, Monday, 7pm – 8:30pm | Audi: 1

Chair: Shyam Dujari, Senior Director, Power Integrations, Inc.

Agenda: This session will open with a perspective on the semiconductor industry's pervasive nature and an insanely deflationary nature unlike any other in the human history! Relative to its size it has an outsized impact on every facet of our individual lives, society, and to the world's energy security and decarbonization.

Fuel that drives semiconductors is the IP creation, and a sustainable world class leadership requires differentiated IP on multiple dimensions in various sub-segments with different skill sets, capital intensity and risk/reward.

Academia can play an important role to mitigate the risk, but a successful outcome needs not only the industry and academia collaboration, but also venture capital, standards bodies, and an enabling environment from the government. Panel discussion will focus on how to achieve this.

Panel:

1. Raja Manickam, CEO, Tata Semiconductor OSAT
2. Saravana Chandran, Chief Technologist, Vitalcore Group

Industry Session – II: India's Best Bets into Chip Technology – Where is the Green Field?
Dec 12th, Monday, 7pm – 8:30pm

Chair: Dr. Amith Singhee, CTO, IBM | Audi: 2

Agenda: India has ambitious aspirations of growing industry and technology leadership in areas such as semiconductors and quantum computing. There are many strategic choices that face industry and government, ranging across semiconductor technology advancement, heterogenous integration, leapfrogging to new technologies such as neuromorphic or quantum electronics. This panel will discuss what and how investments should be prioritised and what are some areas to be avoided.

Panel:

1. Praveen Ganapathy, Director at TI
2. Anand Haridass, Senior Principal Eng., Intel
3. Niranjan Pol, Senior Engineering Director, SeaGate
4. Varsha Kadam, Director – Business Development, Interplex.
5. Ashwath Rao, Senior Research Analyst, Counterpoint.

Industry Session – III: Is India Ready for High Volume Semiconductor Manufacturing?
Dec 13th, Tuesday, 7pm – 8:30pm | Audi: 1

Chair: Dr. Madhur Bobde, CTO, Alpha Omega Semiconductor

Agenda: Despite significant progress in many High-Tech areas in the last few decades, semiconductor manufacturing still eludes India. What are the reasons behind that? This panel will discuss if the factors that were causing this have now changed and whether there are any more hurdles that need to be overcome to achieve High Volume semiconductor manufacturing in India. Some other factor such as explosion of semiconductor demand due to EV, renewable energy and geo-political changes causing countries to secure their semiconductor supply chain will also be discussed

Panel:

1. Mr. Sameer Pendharkar, Vice President, Technology Development & TI Senior Fellow
2. Dr. Primit Parekh, Co-Founder & President, Transphorm Inc
3. Dr. Shekar Mallikarjunaswamy, Vice President IC Technology & TVS, AOS
4. Dr. Ritu Sodhi, Technical Consultant, ROHM Semiconductor, India
5. Dr. Ravi Todi, Sr. Technologist, Western Digital Inc.

Industry Session – IV: Scope of Industry – Academia Collaborations for Scaling PV Manufacturing
Dec 13th, Tuesday, 7pm – 8:30pm | Audi: 2

Chair: Dr. Subramanyam Pulipaka, CEO, National Solar Energy Federation of India (NSEFI)

Agenda: India is moving firmly in the direction of transitioning to a green energy future, and photovoltaics is poised to play a key role in this transition. With ambitious targets for PV deployment Government of India has announced two tranches of Production Linked Incentive (PLI) Scheme with a total outlay of around 3 billion USD aimed at not only serving India's domestic demand but growing Global Appetite for Indian manufactured goods. However, the issues pertaining to skilled workforce and technology remain major impediments for scaling of PV manufacturing in India. The panel would deliberate on the challenges in cell, module, storage, and grid integration and the scope for industry – academia collaborations in these areas.

Panel (Tentative):

1. Mr. Anandi Iyer, Head India Office, ISE Fraunhofer
2. Mr. Sujay Ghosh, Vice President & Country Managing Director, First Solar
3. Mr. Ajay Kapoor, Tata Power Solar
4. Mr. Arul Shanmugasundaram, Executive Director, Ayana Power
5. Mr. Lalit Bohra, Jt. Secretary, MNRE
6. Prof. Ayodhya Tiwari, ETH Zurich
7. Prof. Anil Kottantharayil, IIT Bombay
8. Prof. Sushobhan Awasthi, IISc Bangalore

Young Researcher's Meet (YRM)

12th December 2022, 6:30-8.00pm IST, Audi 8 & 9

Young Researchers Meet is an invitation to young minds to the Women in Semiconductor (WiSemi) session to get inspired brilliant minds leading industry roadmap.

IEEE EDS Young Professional and Meet-n-Greet

14th December 2022, 4:30-6.30pm IST, Audi 11

Session Moderator: Dr. Pragya Kushwaha, IEEE EDS Early Career Awardee

The IEEE Young Professionals (formerly GOLD—Graduates of the Last Decade) is a program to help IEEE members (with at least one engineering-relevant degree) transitioning to young professionals and accomplish their early career goals. Under the umbrella of IEEE, this is a vibrant community of engineers, scientists, and technical experts with representation across the globe, and now the IEEE Electron Device Society (EDS) is further empowering young professionals through the creation of Young Professionals (YP) in IEEE EDS group.

Young Professionals in IEEE EDS is a session to showcase the journeys of a few young minds in the Electron Device Society areas and how IEEE enabled them to succeed in their careers. This will be an in-person/offline networking event, to get mentorship from these Young Professionals to build a successful EDS career with the help of IEEE and the EDS community. The session will be of interest to everyone, but particularly to budding EDS professionals and students who are looking for inspiration.

Event will cover following activities:

- Introduction of Mentors (3 words / 3 sentences)
- EDS Benefits for Young Professionals and Women
- Mentoring & Networking Session

Women in Semiconductor (WiSemi)

12th December 2022, 6:30-8.00 pm IST, Audi 8 & 9

Session Moderator: Prof. P. Susthitha Menon N V Visvanathan, The National University of Malaysia

Women in Semiconductor session is a special session to showcase the inspiring journeys of women leaders in semiconductor. This session over lunch will be a casual session where Seven (Women) Industry leaders will talk about their journey from the macroscopic world to the micro/nanoscopic world and how they emerged as leaders. This session will be of interest to everyone, but particularly to budding semiconductor professionals and students who are looking for inspiration and role models.

Panelists:

1. Ms. Bharathi V, Principal Engineer - Senior Technologist - Platform Power-n-Performance, Intel Corporation
2. Ms. Sushma Nirmala Sambatur, Design Manager, Memory, Global Foundries.
3. Ms. Sumedha Limaye, Vice President of Engineering, Xeon & Networking @ Intel India
4. Dr. Gauri Karve, Senior Project Manager, IMEC
5. Ms. Sneha Revankar, Associate Director Samsung Semiconductor India Research
6. Ms. Bindu Rao, Principal Engineer, Intel Corporation
7. Prof. Merlyne De Souza, Chair in Micro Electronics, The University of Sheffield

Poster Session Details Overview

Audi 3 | 7:00PM - 9:00PM | Day 1 and 2

Track Name	Date	No of Posters
Energy Storage and Batteries (ESB)	12-Dec-22	7
Integrated Photonics & Fibre Lasers (IPFL)	12-Dec-22	4
LED & Semiconductor Lasers: Device, Physics & Modules (LL)	12-Dec-22	3
Macroelectronics & Displays: devices, circuits & systems (DIS)	12-Dec-22	8
MEMS/NEMS and Heterogeneously Integrated Devices (NEMS)	12-Dec-22	5
Sensors and Bioelectronics (SBE)	12-Dec-22	12
Solar Cells & Photodetectors: Physics, Device, & Modules (SP)	12-Dec-22	26
2D Material Based Technologies (2DT)	13-Dec-22	13
Advanced Logic Technologies (ALT)	13-Dec-22	1
Advanced Memory Technologies (AMT)	13-Dec-22	2
Advanced Power Device Technology (APDT)	13-Dec-22	2
Modelling and Simulations (MS)	13-Dec-22	17
Neuromorphic Device Technology, Circuits and Systems (NDTCS)	13-Dec-22	2
Other Emerging Devices & Compute Technology (EDCT)	13-Dec-22	1
Quantum Control & Cryogenic Electronics (QCCE)	13-Dec-22	0
Quantum Device Technologies (QDT)	13-Dec-22	4
Reliability Physics of Semiconductor Devices (RPSD)	13-Dec-22	4
RF, Millimeter and THz Technologies, Circuits and Systems (RF-THz)	13-Dec-22	10
Wide Bandgap Power Semiconductor Technologies (WPSD)	13-Dec-22	3

Technical Session Overview

Track: 2D Material Based Technologies (2DT)
Session No: 1 | Session Title: Applications of 2D materials and devices 1
Session Chair: Prof. Zakaria Al Balushi | Audi: 1 | Date: 12/12/2022 | Start Time: 02:30 PM

Session No: 12 | Session Title: 2D materials for photonics and optoelectronic
Session Chair: Prof. Mario Lanza | Audi: 1 | Date: 12/12/2022 | Start Time: 04:15 PM

Session No: 23 | Session Title: Fundamentals of 2D devices 1
Session Chair: Prof. Yashowanta N Mohapatra | Audi: 1 | Date: 12/13/2022 | Start Time: 11:15 AM

Session No: 34 | Session Title: Fundamentals of 2D devices 2
Session Chair: Prof. Eilam Yalon | Audi: 1 | Date: 12/13/2022 | Start Time: 02:30 PM

Session No: 45 | Session Title: Graphene and related materials
Session Chair: Prof. Luis A Jauregui | Audi: 1 | Date: 12/13/2022 | Start Time: 04:30 PM

Session No: 56 | Session Title: Growth and application of 2D materials
Session Chair: Prof. Saptarshi Das | Audi: 1 | Date: 12/14/2022 | Start Time: 11:15 AM

Session No: 67 | Session Title: Applications of 2D materials and devices 2
Session Chair: Prof. Bent Weber | Audi: 1 | Date: 12/14/2022 | Start Time: 02:30 PM

Session No: 78 | Session Title: Emerging phenomenon in 2D materials
Session Chair: Prof. Prasana K Sahoo | Audi: 1 | Date: 12/14/2022 | Start Time: 04:30 PM

Track: Advanced Logic Technologies (ALT)
Session No: 11 | Session Title: Design Technology Co-Optimization
Session Chair: Dr. Arun Joseph | Audi: 11 | Date: 12/12/2022 | Start Time: 02:30 PM

Session No: 22 | Session Title: Design Automation in Advanced Technologies
Session Chair: Dr. Rahul Rao | Audi: 11 | Date: 12/12/2022 | Start Time: 04:30 PM

Session No: 33 | Session Title: Process Integration and Technology
Session Chair: Prof. Deleep Nair | Audi: 11 | Date: 12/13/2022 | Start Time: 11:15 AM

Session No: 59 | Session Title: Heterogenous Integration : Chiplets and 3D
Session Chair: Dr. Rama Divakaruni | Audi: 4 | Date: 12/14/2022 | Start Time: 11:15 AM

Session No: 70 | Session Title: Advanced Logic Devices
Session Chair: Dr. Julien Ryckaert | Audi: 4 | Date: 12/14/2022 | Start Time: 02:30 PM

Session No: 81 | Session Title: Challenges in Computing Systems
Session Chair: Dr. Rahul Rao | Audi: 4 | Date: 12/14/2022 | Start Time: 04:30 PM

Track: Advanced Memory Technologies (AMT)
Session No: 7 | Session Title: Memories: New Horizons
Session Chair: Prof Shubham Sahay | Audi: 7 | Date: 12/12/2022 | Start Time: 02:30 PM

Session No: 51 | Session Title: Advances in Memory Applications and Modeling
Session Chair: Prof Daniele Ielmini | Audi: 7 | Date: 12/13/2022 | Start Time: 04:30 PM

Session No: 66 | Session Title: Intelligent Memories
Session Chair: Prof Udayan Ganguly | Audi: 11 | Date: 12/14/2022 | Start Time: 11:15 AM

Track: Advanced Power Device Technology (APDT)
Session No: 21 | Session Title: Silicon Stays Strong
Session Chair: Dr. Madhur Bobde | Audi: 10 | Date: 12/12/2022 | Start Time: 04:30 PM

Session No: 32 | Session Title: Advances in Silicon Based Power Devices
Session Chair: Dr. Ritu Sodhi | Audi: 10 | Date: 12/13/2022 | Start Time: 11:15 AM

Session No: 43 | Session Title: Power Electronics Systems and Applications
Session Chair: Prof. Shankar Madathil | Audi: 10 | Date: 12/13/2022 | Start Time: 02:30 PM

Session No: 65 | Session Title: Advances in Power Electronics Circuits
Session Chair: Dr. Sukhendu Deb Roy | Audi: 10 | Date: 12/14/2022 | Start Time: 11:15 AM

Track: Electrostatic Discharge Reliability (ESD)
Session No: 62 | Session Title: On-Chip ESD Devices and Physics
Session Chair: Harshit Dhakad (Intel) | Audi: 7 | Date: 12/14/2022 | Start Time: 11:15 AM

Track: Electrostatic Discharge Reliability (ESD) & ULSI Circuits/System-on-Chip/Power SoC (SoC)
Session No: 18 | Session Title: ESD & SoC Design and Verification
Session Chair: Dr. Rajat Sinha (Micron) | Audi: 7 | Date: 12/12/2022 | Start Time: 04:30 PM

Session No: 42 | Session Title: ESD Devices & SoC Design
Session Chair: Dr. N. S. Kranthi (TI) | Audi: 9 | Date: 12/13/2022 | Start Time: 02:30 PM

Track: Energy Storage and Batteries (ESB)
Session No: 6 | Session Title: Advanced Rechargeable Batteries
Session Chair: Prof. Praveen Ramamurthy | Audi: 6 | Date: 12/12/2022 | Start Time: 02:30 PM

Session No: 17 | Session Title: Photo-Rechargeable and High-Capacity Batteries
Session Chair: Prof. Praveen Ramamurthy | Audi: 6 | Date: 12/12/2022 | Start Time: 04:15 PM

Session No: 28 | Session Title: Electrochemical Mechanism and Interfaces
Session Chair: Dr. Aiswarya Bhaskar | Audi: 6 | Date: 12/13/2022 | Start Time: 11:15 AM

Session No: 72 | Session Title: Metal Air Batteries and Hybrid Energy Storage Systems
Session Chair: Dr. Aiswarya Bhaskar | Audi: 6 | Date: 12/14/2022 | Start Time: 02:30 PM

Track: Integrated Photonics & Fibre Lasers (IPFL)
Session No: 53 | Session Title: Integrated Photonics - Active devices, Programmability and Nonlinearity
Session Chair: Prof. Shankar Selvaraja | Audi: 9 | Date: 12/13/2022 | Start Time: 04:30 PM

Session No: 79 | Session Title: Integrated Photonics - Components and Metamaterials
Session Chair: Prof. Shailendra Varshney | Audi: 2 | Date: 12/14/2022 | Start Time: 04:30 PM

Track: LED & Semiconductor Lasers: Device, Physics & Modules (LL)
Session No: 31 | Session Title: Nitride based optical sources
Session Chair: Prof. Sudharsanan Srinivasan | Audi: 9 | Date: 12/13/2022 | Start Time: 11:15 AM

Session No: 54 | Session Title: Dense laser integration on silicon
Session Chair: Prof. Sudharsanan Srinivasan | Audi: 10 | Date: 12/13/2022 | Start Time: 04:30 PM

Session No: 76 | Session Title: Specialized sources - Lasers & LED
Session Chair: Prof. Kausik Majumdar | Audi: 10 | Date: 12/14/2022 | Start Time: 02:30 PM

Track: LED & Semiconductor Lasers: Device, Physics & Modules (LL) & Integrated Photonics & Fibre Lasers (IPFL)
Session No: 20 | Session Title: Advanced photonic integrated circuits
Session Chair: Prof. Yating Wan | Audi: 9 | Date: 12/12/2022 | Start Time: 04:30 PM

Track: Macroelectronics & Displays: Devices, Circuits & Systems (DIS)
Session No: 16 | Session Title: Materials and Device Application Approaches
Session Chair: Prof. Subho Dasgupta | Audi: 5 | Date: 12/12/2022 | Start Time: 04:30 PM

Session No: 27 | Session Title: OLEDs and Display Technology
Session Chair: Prof. Dinesh Kabra | Audi: 5 | Date: 12/13/2022 | Start Time: 11:15 AM

Session No: 38 | Session Title: Thin Film Transistors

Session Chair: Prof. Sanjiv Sambandan | Audi: 5 | Date: 12/13/2022 | Start Time: 02:30 PM

Session No: 49 | Session Title: Displays: Design, Fabrication,and Processing
Session Chair: Prof. Monica Katiyar | Audi: 5 | Date: 12/13/2022 | Start Time: 04:30 PM

Session No: 60 | Session Title: Sustainable Devices and Systems
Session Chair: Prof. Cantarella Giuseppe | Audi: 5 | Date: 12/14/2022 | Start Time: 11:15 AM

Session No: 71 | Session Title: Flexible and Smart Systems for Digital World
Session Chair: Prof. Shree Prakash Tiwari | Audi: 5 | Date: 12/14/2022 | Start Time: 02:30 PM

Track: MEMS/NEMS and Heterogeneously Integrated Devices (NEMS)
Session No: 52 | Session Title: RF & General MEMS Devices
Session Chair: Prof. Shanti Bhattacharya | Audi: 8 | Date: 12/13/2022 | Start Time: 04:30 PM

Session No: 63 | Session Title: Piezoelectric MEMS
Session Chair: Prof. Dhiman Mallick | Audi: 8 | Date: 12/14/2022 | Start Time: 11:15 AM

Session No: 83 | Session Title: Microfluidics and Bio-sensing
Session Chair: Prof. Prosenjit Sen | Audi: 8 | Date: 12/14/2022 | Start Time: 04:30 PM

Track: Modelling and Simulations (MS)
Session No: 2 | Session Title: Nanoelectronics and Process Modelling
Session Chair: Prof. Nihar Mohapatra | Audi: 2 | Date: 12/12/2022 | Start Time: 02:30 PM

Session No: 13 | Session Title: Compact Modelling, PDK and BiCMOS Process
Session Chair: Prof. Avirup Dasgupta | Audi: 2 | Date: 12/12/2022 | Start Time: 04:15 PM

Session No: 24 | Session Title: High Frequency Measurements and Modelling
Session Chair: Prof. Yogesh Chauhan | Audi: 2 | Date: 12/13/2022 | Start Time: 11:15 AM

Session No: 35 | Session Title: Ferroelectric, Negative Capacitance and Tunnel FET
Session Chair: Prof. Pramod Tiwari | Audi: 2 | Date: 12/13/2022 | Start Time: 02:30 PM

Session No: 64 | Session Title: Machine Learning and Device Modelling
Session Chair: Mr. Srikanth Srihari | Audi: 9 | Date: 12/14/2022 | Start Time: 11:15 AM

Session No: 75 | Session Title: Atomistic Modelling and Simulation
Session Chair: Prof. Avirup Dasgupta | Audi: 9 | Date: 12/14/2022 | Start Time: 02:30 PM

Session No: 84 | Session Title: Multi-scale, 2D and Nanosheet Modelling
Session Chair: Prof. Nihar Mohapatra | Audi: 9 | Date: 12/14/2022 | Start Time: 04:15 PM

Track: Neuromorphic Device Technology, Circuits and Systems (NDTCS)
Session No: 5 | Session Title: Emerging trends in Neuromorphic Computing
Session Chair: Prof. Bipin Rajendran | Audi: 5 | Date: 12/12/2022 | Start Time: 02:30 PM

Session No: 44 | Session Title: Accelerators for Edge Intelligence
Session Chair: Prof. Shubham Sahay | Audi: 11 | Date: 12/13/2022 | Start Time: 02:30 PM

Session No: 55 | Session Title: Emerging memories for Neuromorphic Computing
Session Chair: Prof. Sandip Mondal | Audi: 11 | Date: 12/13/2022 | Start Time: 04:30 PM

Session No: 77 | Session Title: Novel devices for Neuromorphic Computing
Session Chair: Prof. Debanjan Bhowmik | Audi: 11 | Date: 12/14/2022 | Start Time: 02:30 PM

Track: Other Emerging Devices & Compute Technology (EDCT)
Session No: 9 | Session Title: Other Emerging Devices & Compute Technology - 1
Session Chair: Prof. Debanjan Bhowmik | Audi: 9 | Date: 12/12/2022 | Start Time: 02:30 PM

Session No: 41 | Session Title: Other Emerging Devices & Compute Technology – 2
Session Chair: Prof. Nihar Mohapatra | Audi: 8 | Date: 12/13/2022 | Start Time: 02:30 PM
Session No: 74 | Session Title: Other Emerging Devices & Compute Technology – 3

Session Chair: Prof. Shubham Sahay | Audi: 8 | Date: 12/14/2022 | Start Time: 02:30 PM

Track: Quantum Control & Cryogenic Electronics (QCCE)
Session No: 61 | Session Title: Quantum Control & Cryogenic Electronics
Session Chair: Dr. Amith Singhee (IBM) | Audi: 6 | Date: 12/14/2022 | Start Time: 11:15 AM

Track: Quantum Device Technologies (QDT)
Session No: 30 | Session Title: Quantum Device Technologies
Session Chair: Prof. Neeraj Khare (IITD) | Audi: 8 | Date: 12/13/2022 | Start Time: 11:15 AM

Track: Reliability Physics of Semiconductor Devices (RPSD)
Session No: 39 | Session Title: Reliability Physics of Semiconductor Devices – 1
Session Chair: Dr. Shubhakar (SUTD) | Audi: 6 | Date: 12/13/2022 | Start Time: 02:30 PM

Session No: 50 | Session Title: Reliability Physics of Semiconductor Devices - 2
Session Chair: Dr. Pritom Jyoti Bora (SUTD) | Audi: 6 | Date: 12/13/2022 | Start Time: 04:30 PM

Track: RF, Millimeter and THz Technologies, Circuits and Systems (RF-THz)
Session No: 10 | Session Title: THz sensing and Imaging
Session Chair: Dr. S. S. Prabhu | Audi: 10 | Date: 12/12/2022 | Start Time: 02:30 PM

Session No: 29 | Session Title: THz spectroscopy for Materials
Session Chair: Dr. Dibakar Roy Chowdhury | Audi: 7 | Date: 12/13/2022 | Start Time: 11:15 AM

Session No: 40 | Session Title: Technologies for RF/mmwave/THz radio
Session Chair: Dr. Eric Desbonnets | Audi: 7 | Date: 12/13/2022 | Start Time: 02:30 PM

Session No: 73 | Session Title: RF/mmwave/THz Devices and Circuits
Session Chair: Dr. Eric Desbonnets | Audi: 7 | Date: 12/14/2022 | Start Time: 02:30 PM

Session No: 82 | Session Title: RF/mmwave/THz Circuits and systems
Session Chair: Dr. Mh. Rahman | Audi: 7 | Date: 12/14/2022 | Start Time: 04:30 PM

Track: Sensors and Bio-Electronics (SBE)
Session No: 4 | Session Title: Biosensors – 1
Session Chair: Prof. Sameer Sonkusale | Audi: 4 | Date: 12/12/2022 | Start Time: 02:30 PM

Session No: 15 | Session Title: Advanced Sensing
Session Chair: Dr. Kiran Aatre | Audi: 4 | Date: 12/12/2022 | Start Time: 04:30 PM

Session No: 26 | Session Title: Biosensors 2
Session Chair: Prof. Ambarish Ghosh | Audi: 4 | Date: 12/13/2022 | Start Time: 11:15 AM

Session No: 37 | Session Title: Electrochemical Sensors
Session Chair: Prof. Sushmee Badhulika | Audi: 4 | Date: 12/13/2022 | Start Time: 02:30 PM

Session No: 48 | Session Title: Nanomaterials based Sensors
Session Chair: Prof. Praveen Ramamurthy | Audi: 4 | Date: 12/13/2022 | Start Time: 04:30 PM

Track: Solar Cells & Photodetectors: Physics, Device, & Modules (SP)
Session No: 8 | Session Title: Thin-Film Photovoltaics
Session Chair: Dr. Jim John | Audi: 8 | Date: 12/12/2022 | Start Time: 02:30 PM

Session No: 19 | Session Title: Photodetectors
Session Chair: Dr. Gauri Karwe | Audi: 8 | Date: 12/12/2022 | Start Time: 04:15 PM

Session No: 46 | Session Title: New approaches and Advanced Devices
Session Chair: Prof. K. L. Narasimhan | Audi: 2 | Date: 12/13/2022 | Start Time: 04:30 PM

Session No: 57 | Session Title: Photovoltaic Reliability
Session Chair: Prof. Anil Kottantharayil | Audi: 2 | Date: 12/14/2022 | Start Time: 11:15 AM
Session No: 68 | Session Title: Next-Generation of Commercial Solar Technologies

Session Chair: Prof. Dinesh Kabra | Audi: 2 | Date: 12/14/2022 | Start Time: 02:30 PM

Track: Wide Bandgap Device Based Circuits and Systems (WDCS)
Session No: 25 | Session Title: WBG device based Power Electronics Applications
Session Chair: Dr. Kamal Varadarajan | Audi: 3 | Date: 12/13/2022 | Start Time: 11:15 AM

Session No: 58 | Session Title: WBG device based integrated systems and application considerations
Session Chair: Mr. Yoganand Parthasarathy | Audi: 3 | Date: 12/14/2022 | Start Time: 11:15 AM

Session No: 3 | Session Title: Advanced GaN Technologies
Session Chair: Prof. Srabanti Chowdhury (Stanford) | Audi: 3 | Date: 12/12/2022 | Start Time: 02:30 PM

Session No: 14 | Session Title: State of the art Ga2O3 Devices & Physics
Session Chair: Prof. Srabanti Chowdhury (Stanford) | Audi: 3 | Date: 12/12/2022 | Start Time: 04:15 PM

Session No: 36 | Session Title: Process Integration and Technology of Ga2O3 Devices
Session Chair: Dr. Kamal Varadarajan | Audi: 3 | Date: 12/13/2022 | Start Time: 02:30 PM

Track: Wide Bandgap Power Semiconductor Technologies (WPSD)
Session No: 47 | Session Title: GaN and SiC Device Technology & Physics - 1
Session Chair: Dr. Kamal Varadarajan | Audi: 3 | Date: 12/13/2022 | Start Time: 04:15 PM

Session No: 69 | Session Title: GaN and SiC Device Technology & Physics – 2
Session Chair: Dr. Ritu Sodhi | Audi: 3 | Date: 12/14/2022 | Start Time: 02:30 PM

Session No: 80 | Session Title: GaN Device Technology & Physics
Session Chair: Dr. Ritu Sodhi | Audi: 3 | Date: 12/14/2022 | Start Time: 04:15 PM

Poster & Technical Sessions

Session No: 1 | Session Title: Applications of 2D materials and devices 1
Audi: 1 | 02:30 PM-04:15 PM | **Session Chair:** Prof. Zakaria Al Balushi
Track: 2D Material Based Technologies (2DT)
Date: 12-Dec-22

1-1: Logic-in-Memory Based on an Atomically Thin Semiconductor (Invited Talk)
Start Time: 02:30 PM (30 Mins)
Speaker/Author: Prof. Andras Kis, École Polytechnique Fédérale de Lausanne, Switzerland
Presenter: Prof. Andras Kis

Abstract: Machine learning and signal processing on the edge are poised to influence our everyday lives with devices that will learn and infer from data generated by smart sensors and other devices for the Internet of Things. The next leap towards ubiquitous electronics requires increased energy-efficiency of processors for specialized data-driven applications. I will present here how we realised an in-memory processor fabricated using a two-dimensional materials platform can potentially outperform its silicon counterparts in both standard and non-traditional Von Neumann architectures for artificial neural networks. The circuits are based on a flash memory array with a two-dimensional channel using wafer-scale MoS2. Simulations and experiments show that the device can be scaled down to sub-μm channel length without any significant impact on its memory performance.

1-2: Hybrid 2D/CMOS microchips for memristive applications (Invited Talk)
Start Time: 03:00 PM (30 Mins)
Speaker/Author: Prof. Mario Lanza, King Abdullah University of Science and Technology, Saudi Arabia
Presenter: Prof. Mario Lanza

Abstract: Two-dimensional layered materials (2D-LMs) materials have outstanding electronic and thermal properties that make them attractive for the fabrication of solid-state micro/nano-electronic devices and circuits. However, synthesizing high-quality 2D-LMs at the wafer scale is difficult, and integrating them in semiconductor production lines brings associated multiple challenges. In this invited talk, I will discuss the state-of-the-art on micro/nano-electronic devices made (entirely or partially) of 2D-LMs, the most sophisticated circuits ever constructed, and the fabrication of hybrid 2D/CMOS microchips. I will put special emphasis on devices that employ hexagonal boron nitride, the only 2D-LM with an enough high band gap to be employed as dielectric. I will also discuss the main technological challenges to face in the next years and provide some recommendations on how to solve them.

1-3: Integration of Two-Dimensional Memtransistors for Near Sensor Compute and Storage (Oral)
Start Time: 03:30 PM (15 Mins)
Speaker/Author: Shiva Subbulakshmi Radhakrishnan, Akhil Dodda and Saptarshi Das (Pennsylvania State University, USA)
Presenter: Shiva Subbulakshmi Radhakrishnan

Abstract: The close integration of sensing, computing, and storage are quintessential for energy-efficient computing. Unfortunately, current edge devices require cloud servers to perform the necessary computation, leading to latency and unreliability. We have integrated 196 2D MoS2 memtransistor to realize a 7 x 7 pixel edge device capable of sensing, storing, and computing. Our findings highlight the potential of multifunctional 2D materials in developing near-sensor compute and storage capabilities that can overcome the bottleneck of Von Neumann architecture. We have also demonstrated minimal device-to-device performance, accounting for the high quality and uniform MOCVD growth of our 2D material.

1-4: Complex oxide membranes as dielectrics for 2D materials (Invited Talk)
Start Time: 03:45 PM (30 Mins)
Speaker/Author: Prof. Bharat Jalan, University of Minnesota, Twin Cities
Presenter: Prof. Bharat Jalan

Abstract: With a rapidly growing family of vdW materials, the role of dielectric and metals have become more important than ever. In this talk, we will present a detailed synthesis, and characterization of various complex oxide nanomembranes as a high-k dielectric. We will present a detailed growth study of SrTiO3 (STO) nanomembranes. Using hybrid molecular beam epitaxy that employs a metal-organic precursor, titanium isopropoxide (TTIP), to supply both Ti and oxygen (without the need for additional oxygen), epitaxial STO films were grown directly on a graphene layer transferred on to bulk STO substrate. Films were then successfully

exfoliated and transferred onto other substrates. Using Raman spectroscopy and high-resolution X-ray diffraction, we show that the transferred STO membrane is single-crystalline and can be integrated with other vdW materials.

Session No: 2 | Session Title: Nanoelectronics and Process Modelling
Audi: 2 | 02:30 PM-04:15 PM | **Session Chair:** Prof. Nihar Mohapatra
Track: Modelling and Simulations (MS)
Date: 12-Dec-22

2-1: More (than Moore) Electrostatic Doping (Invited Talk)
Start Time: 02:30 PM (30 Mins)
Speaker/Author: Dr. Ray Hueting, University of Twente
Presenter: Dr. Ray Hueting

Abstract: Electrostatic doping is widely emerging as an alternative doping technique to provide high charge carrier densities in nanometer-scale electron devices. In this talk various reported electrostatically doped device architectures and modelling aspects are highlighted. It is shown that in addition to nanometer-scale devices, the electrostatic doping technique can also be effectively utilized in bulk devices especially when elemental metals are replaced by alternative materials, such as transition metal oxides (TMOs) and pure boron. Such materials have a strong potential in, for example, optical and power applications.

2-2: Modeling and Simulation in Semiconductor Processes and Manufacturing (Invited Talk)
Start Time: 03:00 PM (30 Mins)
Speaker/Author: Dr. Samit Barai, Director, Applied Materials, India
Presenter: Dr. Samit Barai

Abstract: As the semiconductor processes are getting more complex, the role of modeling and simulation is becoming more important. Semiconductor process technology development faces many challenges through multiple phases of material selection process, selection of unit processes and process integration options and through multiple production cycles. The challenge for the process development is to attain nanometer level accuracy in a meter scale chamber where chemical bonds are formed in picoseconds but process runs for minuets. Different class of models are used at different levels of process definition and development. The challenges and the advantages of these models in solving high value problems in process development and manufacturing will be discussed in this presentation.

2-3: Process Modeling as a Powerful Semiconductor Industry Tool: PVD of W as Case Study (Oral)
Start Time: 03:30 PM (15 Mins)
Speaker/Author: Piyush Navinchandra Bhatt (Applied Materials India Pvt. Ltd, India); Wei Lei and Shirish Pethe (Applied Materials Inc. Santa Clara CA USA, USA); Rajesh Sathiyanarayanan (Applied Materials India Pvt. Ltd., India); Phillip Stout (Applied Materials Inc. Santa Clara CA USA, USA)
Presenter: Piyush Navinchandra Bhatt

Abstract: This work demonstrates the power of process modeling in semiconductor industry by building a kinetic Monte Carlo (kMC) method-based process model for physical-vapour-deposition (PVD) of Tungsten (W) material inside trench structure. The material properties-based simulation knobs (diffusivity, sticking coefficient, sputtering/yield coefficient and energy) were scanned to calibrate process model to experimental data. Based on the calibrated process model, a GUI based platform was developed, which will help process engineers to simulate deposition profiles and subsequently, optimize their recipes to get desired etch/deposition profiles with reduced time, cost and effort.

2-4: Nano-Electronic Simulation Software (NESS): An Overview (Invited Talk)
Start Time: 03:45 PM (30 Mins)
Speaker/Author: Dr. Tapas Dutta, University of Glasgow, UK
Presenter: Dr. Tapas Dutta

Abstract: In this talk, I'll provide an overview of the new device simulator NESS (Nano-Electronic Simulation Software) developed by the University of Glasgow's Device Modelling Group. It is a fast and modular TCAD tool with flexible architecture and has been implemented in C++. It has its own structure and mesh generation capabilities, and contains different modules including classical, semi-classical, and quantum transport solvers, mobility calculation, kinetic Monte-Carlo and others. NESS can also consider various sources of statistical variability in nanoscale devices and can perform simulations of large number of microscopically different devices

created by the structure generator. I'll summarize the workings of the different modules and demonstrate of the capabilities of NESS by presenting results obtained from the simulation of state-of-the-art and emerging devices.

Session No: 3 | Session Title: Advanced GaN Technologies
Audi: 3 | 02:30 PM-04:15 PM | **Session Chair:** Prof. Srabanti Chowdhury (Stanford)
Track: Wide Bandgap Power Semiconductor Technologies (WPSD)
Date: 12-Dec-22

3-1: III-N mm-Wave Transistors for Linearity, Efficiency, and Reconfigurability (Invited Talk)
Start Time: 02:30 PM (30 Mins)
Speaker/Author: Prof. Patrick Fay, University of Notre Dame, USA
Presenter: Prof. Patrick Fay

Abstract: Achieving the vision and promise of millimeter-wave wireless communication systems (e.g. 6G and beyond) requires significant advancements in device technologies. To obtain the high bandwidths required on a mobile platform, devices offering millimeter-wave performance with low power consumption while simultaneously delivering low noise figure, high linearity, and high power efficiency are essential. Reconfigurability in order to support frequency-agile and compact implementations is also critical. The unique properties of the III-N material system (e.g. polarization, LO phonon mediated electron transport) enable new approaches for designing millimeter-wave transistors for power amplifiers, low-noise amplifiers, and signal switching and routing. The integration of ferroelectrics with III-N transistors also provides opportunities for increased functional density and improved performance in signal switching and routing applications. In this talk, recent advances in these areas will be presented.

3-2: Ultrawide bandgap CMOS platform for heterogenous integration (Invited Talk)
Start Time: 03:00 PM (30 Mins)
Speaker/Author: Prof. Xiaohang Li, KAUST, Saudi Arabia
Presenter: Prof. Xiaohang Li

Abstract: In this talk, I will discuss our latest work of demonstrating the ultrawide bandgap CMOS for heterogeneous integration along with our works of UWBG materials, physics, and devices.

3-3: Physics-Based Approach for Mitigation of Dynamic RON in AlGaN/GaN HEMTs With C-Doped Buffer (Oral)
Start Time: 03:30 PM (15 Mins)
Speaker/Author: Sayak Dutta Gupta, Vipin Joshi and Rajarshi Roy Chaudhuri (Indian Institute of Science, India); Mayank Shrivastava (Indian Institute of Science Bangalore, India)
Presenter: Sayak Dutta Gupta

Abstract: We report a unique stress time and device design dependent OFF-state drain-to-source critical stress voltage, above which the dynamic RON of AlGaN/GaN HEMTs is significantly deteriorated. Detailed experiments reveal channel electric field-controlled electron trapping in carbon-doped GaN buffer to be the source of the dynamic RON. Based on the gained physical insights, a novel p-type AlTiO based surface passivation scheme is demonstrated to mitigate the dynamic RON in the GaN HEMTs.

3-4: NexGen Vertical GaN™ Fin-JFET: Fast Switching and Exceptional Robustness (Invited Talk)
Start Time: 03:45 PM (30 Mins)
Speaker/Author: Dr. Subhash Pidaparthi, NexGen Power Systems
Presenter: Dr. Subhash Pidaparthi

Abstract: We present the results of NexGen's 700V and 1200V normally-off vertical GaN Fin-JFETs. The transistors exhibit small switching losses with no reverse recovery. Switching at 3MHz+ and 1200V is demonstrated. The device can sustain a single-pulse critical avalanche energy density of 10J/cm2 (highest reported in GaN transistors) and >3500 repetitive avalanche pulses. The avalanche current path can be tuned through the gate or the source. The short-circuit withstanding time of 700V Fin-JFETs is 30.5μs at a VBUS of 400V and 11.6μs at 800V, all among the longest reported for 600-700V normally-off transistors. In repetitive 400V/10µs short-circuit tests, Fin-JFETs showed no degradation after 30,000 cycles. These results set a record for GaN transistors and demonstrate equivalent to superior robustness compared to Si and SiC devices.

Session No: 4 | Session Title: Biosensors - 1
Audi: 4 | 02:30 PM-04:00 PM | **Session Chair:** Prof. Sameer Sonkusale
Track: Sensors and Bio-Electronics (SBE)
Date: 12-Dec-22

4-1: Toward the Next Generation of Wearables for Health Monitoring (Invited Talk)
Start Time: 02:30 PM (30 Mins)
Speaker/Author: Prof. Shideh Kabiri Ameri, Queen's University, Canada
Presenter: Prof. Shideh Kabiri Ameri

Abstract: Wearable electronics are a group of electronic devices and sensors with broad applications in mobile health care, Internet of Things (IoT) and Human Machine Interfaces (HMI). Nanomaterials possess extraordinary, electrical, chemical, optical and mechanical properties that can be utilized for the development of the next generation of wearables. In this talk a group of nano materials based non-intrusive wearables with superior performance and visual imperceptibility and their applications for electroencephalography (EEG), electrocardiography (ECG), electromyography (EMG), Electrooculography (EOG), sensing skin temperature and hydration, human machine interface and IoT will be presented.

4-2: Low Voltage Metal Oxide TFT With Back-Contacted Piezoelectric PVDF-HFP Coating for Pressure Sensing Applications (Oral)
Start Time: 03:00 PM (15 Mins)
Speaker/Author: Utkarsh Pandey (IIT (BHU) Varanasi, India); Nila Pal (IIT BHU Varanasi, India); Bhola Pal (IIT (BHU), Varanasi, India)
Presenter: Utkarsh Pandey

Abstract: Li-Alumina (LA) Ion-conducting dielectric thin-film has been prepared through the low-cost sol-gel method and is prosperously use to fabricate the metal-oxide based thin-film transistor (MOTFT). This MOTFT shows the high device performance at very low operating voltage (2V). Li-Alumina thin-film shows a very high insulating nature due to the high band-gap of the material. Furthermore, because of the Li + ion conduction a thin-film LA, can be has a very high areal capacitance and may be used as a gate dielectric for low operating voltage metal-oxide TFTs. Besides, thin-film of LA gives low surface roughness due to its amorphous nature resulting decrease in the gate leakage current in TFT. Also, Li-Alumina dielectric has strong compatibility with the SnO2 semiconducting channel in TFT. A SnO2 thin-film has been deposited on the top of the Li-Alumina dielectric layer by the solution-processed technique in the top contact bottom gate TFT architecture that works as semiconductor channel of the device. To saturate the drain current in this TFT, only 2.0 V or less drain voltage (VD) is required, with a gate bias of 2.0 V. The obtained value of threshold voltage(Vth), carrier mobility (μ) and On/Off ratio of this device are 0.9 V,-1 cm 2 V -1 s -1 and-1.-1 x 10 2 . For the application of this TFT as pressure sensor, a piezoelectric material (PVDF-HFP) thin-film has been fabricated on the top of the device, that works as a back gate in the device. Channel current of this TFT can be modulated by applying pressure on the PVDF-HFP thin-film. Hence, this device works as piezoelectric back-contacted TFT that can also be considered TFT as a pressure sensor. Additionally, this metal-oxide based pressure sensor shows excellent performance in terms of the sensitivity, linearity and response time of the device.

4-3: Smart Textile Materials for Monitoring ECG Signals (Oral)
Start Time: 03:15 PM (15 Mins)
Speaker/Author: Subashini Jm (Indian Institute of Information Technology Design and Manufacturing (IIITDM) Kancheepuram, India)
Presenter: Subashini Jm

Abstract: Smart textiles play a significant role in wearable devices for monitoring the physiological parameters of the human body, such as heart rate, temperature, pressure, etc. The electrocardiograph (ECG) is the most used heart diagnostic tool that records the heart's electrical signals (heart rhythm). The current ECG electrodes used in the hospital for ECG signals are wet electrode types that use Ag/AgCl gel electrodes. Here the Ag/AgCl gel-type electrode sticks on the human skin for an extended period until the ECG reading is wholly taken. The gel used is disposable, sticky, and does not feel comfortable for the user's long-term monitoring. This research has been made to develop ECG electrodes with textile materials. Here the 12-lead ECG was reduced to a 3-electrode system. Two different types of conductive textile materials were used to create electrodes. The nylon yarn coated with the Silver nanoparticle and two-ply yarn of nylon coated with Stainless Steel nanoparticle is taken for the development of conducting material. The conductive yarn is stitched into the cotton fabric using the lock stitch method. The readings were taken by placing the commercial and the textile electrodes parallel on the right arm, left arm, and

right leg readings are recorded. The material's morphological structure and surface roughness are analyzed using SEM, and XRD is used to analyze the material's crystallinity. The yarn is tested for its anti-microbial property to investigate the material's biocompatibility. For silver yarn case, the voltage range is -0.4V to 1.2 V, whereas, for stainless steel, the voltage range is from -0.4V to 0.7V. That implies silver yarn is relatively more sensitive than stainless steel yarn for detecting ECG signals.

4-4: Integrated sensors in precision medecine and agriculture (Invited Talk)
Start Time: 03:30 PM (30 Mins)
Speaker/Author: Prof. Khaled Nabil Salama, King Abdullah Univeristy of Science and Technology, Saudi Arabia
Presenter: Prof. Khaled Nabil Salama

Abstract: In this talk we will present the design and implementation of monolithic and hybrid sensors using integrated circuits. We will show case two examples in precision medecine and agriculture. First, we present a plant-wearable electrochemical sensor for in situ detection of salicylic acid. The sensor utilizes microneedle-based electrodes that are functionalized with a layer of salicylic acid selective magnetic molecularly imprinted polymers. In addition we will present a laser-scribed graphene (LSG) sensors coupled with gold nanoparticles (AuNPs) as a stable promising biosensing platform. This Point of care (PoC) device is highly demanding to control current pandemic, originated from severe acute respiratory syndrome Coronavirus 2 (SARS-CoV-2).The sensor was integrated to a homemade and portable potentistat device, wirelessly connected to a smartphone having a customized application for easy operation.

Session No: 5 | Session Title: Emerging trends in Neuromorphic Computing

Audi: 5 | 02:30 PM-04:15 PM | **Session Chair:** Prof. Bipin Rajendran
Track: Neuromorphic Device Technology, Circuits and Systems (NDTCS)
Date: 12-Dec-22

5-1: Brain-like self-assembled top-down networks in Ag-BN memristive systems (Invited Talk)
Start Time: 02:30 PM (30 Mins)
Speaker/Author: Dr. Pavan Nukala, Indian Institute of Science
Presenter: Dr. Pavan Nukala

Abstract: Brain is an interconnected and complex network of neurons and synapses operating at self-organized criticality (SOC), which enables it to analyze information from noisy and unstructured data with very low power consumption. SOC is characterized by scale free and correlated electrical avalanche activity. We show that a system comprising of CVD grown multilayer hexagonal Boron Nitride (hBN) films contacted with Silver (Ag), can uniquely host two different self-assembled networks both poised at self-organized at criticality (SOC). This system shows bipolar resistive switching between HRS and LRS, each of microstructurally form different classes of networks. External voltage can tune these networks can be tuned from one to another. Our system provides a unique CMOS compatible 2D materials platform hosting neuromorphic networks. Strategies such as reservoir computing can be used to perform tasks with these networks.

5-2: Phase change photonics and interfacing it with electronics for emerging AI hardware (Invited Talk)
Start Time: 03:00 PM (30 Mins)
Speaker/Author: Prof. Harish Bhaskaran, University of Oxford, UK
Presenter: Prof. Harish Bhaskaran

Abstract: As the race towards new hardware that goes beyond the non-von Neumann processor for applications in machine learning and artificial intelligence heats up, photonics is emerging as a promising contender. It is clear that a future solution will have to embed elements that involve both photonics and electronics, ideally within the same chip. In this talk, I will cover fundamental research on device concepts using functional materials that underpin many of the developments over the last decade and present some of our recent work in this area.

5-3: Investigating Various Adder Architectures for Digital In-Memory Computing Using MAGIC-Based Memristor Design Style (Oral)
Start Time: 03:30 PM (15 Mins)
Speaker/Author: Chandan Kumar Jha (German Research Centre for Artificial Intelligence (DFKI) Bremen, Germany); Alireza Mahzoon (University of Bremen, Germany); Rolf Drechsler (University of Bremen/DFKI, Germany)
Presenter: Chandan Kumar Jha

Abstract: Adders are implemented using a wide variety of architectures. These architectures have been extensively studied for digital IC-based implementations. In recent years, in-memory computing has gained interest owing to the benefits it provides in terms of both energy and performance as compared to conventional von Neumann computing. In this work, we for the first time investigate various adder architectures for in-memory computing using the memristor aided logic (MAGIC) design style for memristors. We analyze seven different adder architectures for bit-widths: 8-bit, 16-bit, 32-bit, and 64-bit. We have used the state-of-the-art SIMPLER tool for performing the mapping of these adders to memristor crossbars. We show that serial prefix adders are better suitable for IMC using the MAGIC design style as compared to the widely used ripple carry adder. The adder designs and the mapping will be made open source at https://github.com/agra-uni-bremen/icee2022-magic-adder-lib, to promote further research in the direction.

5-4: Reliability aware CMOS neuromorphic circuits (Invited Talk - Withdrawn)
Start Time: 03:45 PM (30 Mins)
Speaker/Author: Dr. Nilesh Goel, BITS Pilani Dubai Campus, UAE
Presenter: Dr. Nilesh Goel

Abstract: Neuromorphic circuits are gaining popularity due to their application in ANNs. These circuits have low power consumption, better prediction accuracy and are faster than conventional Von-Newman architecture based circuits. The spiking events are really very important in these circuits. Any deviation in spiking may can cause mis communication and led to false prediction. There are certain blocks identified in the neuron circuits which are highly sensitive to degradation. This can cause faulty spiking, positional shift in spiking etc. By mitigating the impact of reliability on those circuit we can minimize the impact of device reliability and hence can make our neuron more reliable.

Session No: 6 | Session Title: Advanced Rechargeable Batteries

Audi: 6 | 02:30 PM-04:15 PM | **Session Chair:** Prof. Praveen Ramamurthy
Track: Energy Storage and Batteries (ESB)
Date: 12-Dec-22

6-1: Solvating Ionic Liquids to Improve Ionic Transport in PEO-based electrolytes (Invited Talk)
Start Time: 02:30 PM (30 Mins)
Speaker/Author: Prof. Elie Paillard, Politecnico di Milano
Presenter: Prof. Elie Paillard

Abstract: PEO derivatives are currently used as electrolytes for Li metal batteries. Despite their advantages, their conductivity at low temperature is low but can be improved by using ionic liquid as plasticizers. To do so, ionic liquids made of an organic cation and a low coordinating anion are typically used. However, since neither low coordinating anions, nor regular cations interact with the Li+ cation, the fraction of the current effectively transported by Li+ is low. Thus, we propose the use of more coordinating anions or even solvating cations to improve ionic transport. This approach not only allows improving Li+ transport, but also the transport of divalent ions such as Ca2+ as investigated within the VIDICAT project (EU: 829145).

6-2: Our Recent Efforts Towards Two Electrode Solar Batteries: Possibilities & Challenges (Invited Talk)
Start Time: 03:00 PM (30 Mins)
Speaker/Author: Dr. Tharangattu Narayanan Narayanan, Tata Institute of Fundamental Research - Hyderabad
Presenter: Dr. Tharangattu Narayanan Narayanan

Abstract: Layered solids are known for their applications in metal ion batteries. In particular, two-dimensional (2D) layered materials are identified as promising candidates for different types of energy devices and optoelectronics. The high surface area and hence the large accessible interaction volume make them suitable for such applications. On another note, new ways of storing solar energy is of high interest due to the importance of renewable energy harvesting and storage. In that context, two electrode solar battery is an emerging concept, where one can store the solar energy directly in to an electrochemical battery storage systems. This solar battery is one having two electrodes but can charge the battery using light without coupling to a solar cell. Some such batteries have shown in the very recent past but their stability for large charge-discharge cycles, mechanism of metal ion battery charging, scalability, efficiency etc are still in question. In this talk, I will be discussing some such issues and our recent efforts in these directions. Our recent findings on an atomic layer, MoS2 for developing a solar battery will be discussed initially. A lithium (Li) ion battery is shown to be rechargeable using the photo-physics happening at the MoS2/MoOx heterostructure electrode of a Li anode based two electrode cell (half cell). This brings promises in developing stable solar batteries of high photoefficiency. This idea has been further

extended to different other possible battery systems where a battery full cell can be realized. The key findings of those works will be discussed during the talk.

6-3: Towards Advanced Rechargeable Metal (Zn, Li)-Air (O2) Battery Systems Using Electrode and Electrolyte Engineering (Oral)
Start Time: 03:30 PM (15 Mins)
Speaker/Author: Pallavi Thakur (Tata Institute of Fundamental Research Hyderbad, India); Tharangattu Narayanan Narayanan (TIFR Hyderabad, India)
Presenter: Pallavi Thakur

Abstract: Utilizing a diverse mix of batteries in electric vehicles (EVs) is estimated to boost the transition to clean and fossil-free cost-effective transportation. This discussion is mainly on the advancement of a 'next-generation' energy storage system called- Metal-Air Batteries (MABs) by overcoming various performance-limiting issues related to their electrodes and electrolytes, where MABs are identified as one of the important elements of next-generation traction. This study highlights the significance of engineering the electrodes and electrolytes for improving the cyclability of MABs with low overpotential for charging. Different strategies set out here open a plethora of new routes in designing high-performance MAB systems by simple tweaking of electrodes/electrolytes.

6-4: Energy Efficient Separations Using Nanoporous Membranes (Invited Talk - Withdrawn)
Start Time: 03:45 PM (30 Mins)
Speaker/Author: Dr. Deepu J. Babu, IIT Hyderabad, India
Presenter: Dr. Deepu J. Babu

Abstract: Separation processes alone account for about 10 – 15 % of global energy consumption. Most of the currently established separation processes are extremely energy intensive and were developed when energy and emissions were not considered to be significant parameters in choosing a particular process. Over the last two decades, the field of separation science has witnessed significant advancements thanks to the development of various nanoporous materials. In this talk, the development of nanoporous membranes based on metal-organic frameworks as well as 2D materials like graphene and graphyne for various separation applications will be discussed.

Session No: 7 | Session Title: Memories: New Horizons

Audi: 7 | 02:30 PM-04:15 PM | **Session Chair:** Prof Shubham Sahay
Track: Advanced Memory Technologies (AMT)
Date: 12-Dec-22

7-1: DNA based electrically readable high-density read only memory array (Invited Talk)
Start Time: 02:30 PM (30 Mins)
Speaker/Author: Prof. M. P. Anantram, University of Washington, USA
Presenter: Prof. M. P. Anantram

Abstract: We will discuss the concept of an electrically readable memory where the logic states are stored in the resistance of double stranded DNA [1]. These memory elements can in principle be connected to bit and word line nanowires fabricated using DNA origami [2]. We will discuss our effort in modeling the conductance of DNA and the performance metrics of a memory array formed using DNA memory elements. As origami nanowires with a high conductance are yet to be fabricated, we will model the array performance for a variety of interconnect resistances ranging from those of carbon nanotubes to much higher resistances. We will end the talk by discussing the challenges that need to be overcome to realize the proposed memory array. [Work done in collaboration with Professors Das, Hihath, Ke, Kubendran, Oren and our students via an SRC grant and NSF Grant Numbers 1807391 (SemiSynBio Program) and 2036865 (Future of Manufacturing).]

[1] Arpan De, Hashem Mohammed, Yiren Wang, Arindam K. Das, M. P. Anantram, Performance Analysis of DNA Crossbar Arrays for High-Density Memory Storage Applications, In review

[2] Joshua Hihath, M. P. Anantram, Yonggang Ke, Nucleic acid-based electrically readable, read-only memory, US Patent App. 17/253,088, 2022.

7-2: Effect of Temperature Induced Phase Variation in ALD TiO2 Dielectric on the Switching Behaviour of RRAM Devices (Oral)

Start Time: 03:00 PM (15 Mins)
Speaker/Author: Anurag Dwivedi, Shalu Saini and Anil Lodhi (Indian Institute of Technology Jodhpur, India); Harshit Agarwal (Indian Institute of Technology Jodhpur, USA); Shree Prakash Tiwari (Indian Institute of Technology Jodhpur, India)
Presenter: Anurag Dwivedi

Abstract: The improvement in performance of the resistive memory device with change in phase of insulating layer due to different deposition temperatures is investigated. The active switching layer TiO 2 was deposited by Atomic Layer Deposition (ALD) at 150 ◦ C, 180 ◦ C and 200 ◦ C to obtain amorphous, lower crystalline order, and higher crystalline order switching medium. All the devices have shown good switching characteristics but with varied endurance variability. The device with TiO 2 deposited at 180 ◦ C is giving better performance with current on/off ratio of ≥10 3, stable retention for 10 2 seconds and lower cycle-to-cycle variability. This work reports a technique to lower the cycle-to-cycle variation without introducing additional fabrication steps.

7-3: Enhanced Remnant Polarization (>70 μC/cm2) at Low Field and Low Processing Temperatures in ALD Grown Ferroelectric Hf0.5Zr0.5O2 (Oral)
Start Time: 03:15 PM (15 Mins)
Speaker/Author: Md Hanif Ali, Rowtu Srinu, Paritosh Meihar, Adityanarayan Pandey, Manoj Yadav, Sandip Lashkare and Udayan Ganguly (Indian Institute of Technology Bombay, India)
Presenter: Md Hanif Ali, Rowtu Srinu

Abstract: Hafnium oxide (HfO2) based ferroelectrics have gained significant attention as non-volatile ferroelectric random-access memories (FeRAM) due to its scalability and integrability in complementary metal oxide semiconductor (CMOS). To enable large scale FeRAM with CMOS integration, a large polarization at low temperature processing and low electric field is essential. Various reports show high polarization at the cost of high processing temperature and higher electric fields. In this paper, we report a low field (3.14 MV/cm) and large polarization (2Pr ~72 μC/cm2) in atomic layer deposition (ALD) grown (at 200 o C) ferroelectric Hf0.5Zr0.5O2 (HZO) thin film at lower post metallization annealing at 600 o C. We discuss the impact of the source of oxygen from H2O precursor in ALD process in creating O-vacancies during deposition with X-Ray diffraction analysis (XRD). Then we discuss the role of low thermal expansion coefficient of tungsten (W) as top and bottom electrode to induce in-plane tensile strain during annealing to enhance orthorhombic phase (o-phase) - essential to get high polarization. A high dielectric constant εr ~42 at -3V shows the improved quality of the ferroelectric film. Finally, we discuss the impact of electric field and frequency on the polarization.

7-4: A Multifaceted Molecular Memristor (Oral)
Start Time: 03:30 PM (15 Mins)
Speaker/Author: Santi Prasad Rath, Sreetosh Goswami and Sreebrata Goswami (Indian Institute of Science, India)
Presenter: Santi Prasad Rath

Abstract: Molecular memristor comprising a Ru-coordinated bis ligated complex has been designed. Depending on different operating conditions such as Voltage and temperature, its current-voltage characteristics changes gradually. Whereas the voltage helps to achieve different molecular conductance states, temperature variation from 300K to 4K can control various supramolecular dynamical components. Imposing different operating conditions can lead to practically all the possible memristive functionalities starting from bipolar, unipolar, volatile, non-volatile, ternary, and binary responses with gradual analog and sharp digital transitions as well as diode characteristics. A mathematical model comprising of multiple parameter design space has been constructed to model all these characteristics.

7-5: Cryogenic Memory Technologies for Quantum Computing and Beyond (Invited Talk - Withdrawn)
Start Time: 03:45 PM (30 Mins)
Speaker/Author: Prof. Ahmedullah Aziz, University of Tennessee, Knoxville, USA
Presenter: Prof. Ahmedullah Aziz

Abstract: Cryogenic memory devices, capable of operating below 4 Kelvin (K) temperature, are widely sought after in both classical and quantum computing paradigms. Most room-temperature memory devices remain functional at/below 4 K. However, the cryogenic environment allows harnessing exotic quantum effects (e.g., superconductivity, topological states) to design unique memory cells. These inherently cryogenic entities provide far superior performance compared with their conventional counterparts. The surging interest in quantum computing, space electronics, high-performance computing, and superconducting circuits has led to rapid

developments in cryogenic data storage technology. This talk provides an overview of the existing and emerging cryogenic memory cells based on superconducting, non-superconducting, and hybrid technologies

Session No: 8 | Session Title: Thin-Film Photovoltaics
Audi: 8 | 02:30 PM-04:15 PM | **Session Chair:** Dr. Jim John
Track: Solar Cells & Photodetectors: Physics, Device, & Modules (SP)
Date: 12-Dec-22

8-1: Thin film photovoltaic technologies: new trends, progress, opportunities and industrial challenges (Invited Talk)
Start Time: 02:30 PM (30 Mins)
Speaker/Author: Prof. Ayodhya Nath Tiwari, Empa-Swiss Federal Laboratories for Materials Science and Technology
Presenter: Prof. Ayodhya Nath Tiwari

Abstract: Thin film solar cells based on Cu(In,Ga)Se2 (called CIGS) and organic-inorganic hybrid Perovskite semiconductors have shown remarkably high photovoltaic conversion efficiencies on glass and flexible substrates in "monofacial", "bifacial", and "tandem" configurations. The trends of progress suggests efficiencies beyond 30% are within reach quite soon. Thin film photovoltaic (PV) technologies show great potential for low cost manufacturing and some specific features of solar modules are especially attractive for terrestrial and space applications. These technologies, different from Si wafer based technologies, offer new opportunities to industries but also pose various challenges. The talk will present status of technologies, emerging trends, and discuss the challenges and opportunities for industries.

8-2: Antisolvent Effect on Acetamidinium Substituted 2D Ruddlesden-Popper Semi-Transparent Perovskite Solar Cells (Oral)
Start Time: 03:00 PM (15 Mins)
Speaker/Author: Vani Pawar (Indian Institute of Sciences Bangalore, India); Anuj Kumar Palariya (Indian Institute of Science Bangalore Karnataka, India); Nisheka Anadkat (Indian Institute of Science, Bangalore, India); Bhumika Sharma (Indian Institute of Science Bangalore Karnataka, India); Sandeep Kumar (IISc Bangalore, India); Sushobhan Avasthi (Indian Institute of Science & Centre for Nano Science and Engineering (CeNSE), India)
Presenter: Vani Pawar

Abstract: Here, we report acetamidinium substituted 2D Ruddlesden-Popper (RP) metal-halide perovskite: (PEA)2(MA(1-x)AAx)n-1PbnI3n+1 (PEA: phenylethylammonium, MA: methylammonium, AA: acetamidinium, x = 0 and 0.1, and n = 2). We investigate the impact of antisolvent chlorobenzene (CB) on the structural, optical, and photovoltaic properties of 2D perovskite solar cells (PSCs). Antisolvent-treated perovskite films are uniform, polycrystalline, continuous, and with a blended texture. The structural and optical investigations suggest that n = 2 ((PEA)2MAPb2I7 and (PEA)2(MA0.9AA0.1)Pb2I7) films manifest the triclinic crystal structure with tunable optical bandgap ranges from 2.08 to 2.13 eV, making it suitable for semi-transparent solar cells. The champion PSC based on (PEA)2(MA0.9AA0.1)Pb2I7 yields a power conversion efficiency of 0.66% with an average visible transmittance (AVT) of 36% and a short-circuit current density (Jsc) of 3.80 mA/cm2. This device's open-circuit voltage (Voc) and fill-factor (FF) are 0.56 V and 30%, respectively. The considerable semitransparency of these devices makes them a potential applicant for building-integrated photovoltaics (BIPV).

8-3: Various Spectral Responses Correlated Performance of Perovskite Solar Cells (Oral)
Start Time: 03:15 PM (15 Mins)
Speaker/Author: Bidisha Nath, Kumar MP, Praveen C Ramamurthy and Debiprosad Roy Mahapatra (Indian Institute of Science, India); Gopalkrishna Hegde (IISc, India)
Presenter: Bidisha Nath, Kumar MP

Abstract: Methylammonium lead iodide is a material with a broad absorption spectrum and interesting emission properties as well as defect physics. Defects in the absorber layer have different activation energy. So, keeping in mind the difference in behavior at different wavelengths corresponding to a different energy, the performance of the n-i-p structured devices along with frequency and voltage-dependent capacitive behavior variation were analyzed at the different parts of the solar spectrum. The difference in charge carrier generation, extraction, and accumulation have been observed for the devices with varying wavelengths. A brief overview of the photoluminescence behavior has also been obtained from excitation wavelength varying experiments.

8-4: Simulation of CsGeI3-Based Perovskite Solar Cells Using Graphene Oxide Interfacial Layer for Improved Device Performance (Oral)
Start Time: 03:30 PM (15 Mins)
Speaker/Author: Abhijit Das (PDPM-IIITDM, Jabalpur, India); Dip Prakash Samajdar (PDPM IIITDM Jabalpur, India)
Presenter: Abhijit Das

Abstract: In this paper, we have investigated the effect of the Graphene Oxide (GO) interfacial layer (IL) inserted between the absorber layer and Electron Transport Layer (ETL) in lead (Pb)-free all inorganic CsGeI3-based perovskite solar cells (PSCs) using solar cell simulator capacitance software (SCAPS-1D). The performance parameters of the FTO/TiO2/GO/CsGeI3/P3HT PSC device structure have been studied thoroughly, by changing the thickness of the active layer and IL, bulk defect density with defect energy levels of the absorber layer, band gap variation of the Graphene Oxide thin film and the variation of shunt and series resistance. It has been found that the introduction of GO interlayer in the PSC improved the device efficiency by ~ 6%. This is mainly due to the passivation of trap states (i.e. reducing charge recombination and ion migration), efficient band alignment and improved charge injection at the Perovskite/ETL interface. We have reported an optimized power conversion efficiency (PCE) (%) value of 20.03% for the proposed device structure and observed a remarkable improvement in performance parameters.

8-5: Progress, Challenges and Prospects with CdTe Photovoltaics Technology (Invited Talk)
Start Time: 03:45 PM (30 Mins)
Speaker/Author: Prof. Amit Munshi, Colorado State University
Presenter: Prof. Amit Munshi

Abstract: CdTe-based PV technology has evolved from being an “interesting material experiment” to a commercially viable and successful PV solution over the past 20 years. Owing to the ease of manufacturing, material availability and utilization, and inherent tolerance to defects the research efforts have provided rich returns. In this talk, the various improvements in device structure and the fundamental understanding of the material properties that led to improvement in performance will be discussed. Future trajectories for improvement in performance and possible causes for efficiency improvements beyond 22% record efficiency will also be discussed. In addition to these aspects, questions pertaining to material availability and safety will be addressed. The aim is acquaint the audience with the progress, challenges and prospects of CdTe PV technology.

Session No: 9 | Session Title: Other Emerging Devices & Compute Technology - 1

Audi: 9 | 02:30 PM-04:15 PM | **Session Chair:** Prof. Debanjan Bhowmik
Track: Other Emerging Devices & Compute Technology (EDCT)
Date: 12-Dec-22

9-1: Modelling of charge and spin transport in magnetic heterostructures of topological insulators (Invited Talk)
Start Time: 02:30 PM (30 Mins)
Speaker/Author: Dr. Rik Dey, Department of Electrical Engineering, Indian Institute of Technology Kanpur, India
Presenter: Dr. Rik Dey

Abstract: The discovery of spin-orbit coupling (SOC) in different materials have revolutionized the area of spintronics which relies on both the charge and spin degrees of freedom of an electron. Materials with high SOC can be utilized for efficient transduction between charge and spin currents that can be used for low-power switching of nano-magnetic bits, which will lead to the next-generation spin-orbit torque (SOT) based memory devices. In this regard, a new class of materials called topological insulators (TIs) are the ideal ones for such SOT-based devices because of a near-perfect spin-charge interconversion efficiency achievable on the surface of a TI. In this talk, I will present a detailed theoretical modelling of the coupled charge and spin transport in magnetic heterostructures comprising of these TI materials.

9-2: "Topo-tronic" device modeling- Proposal for steep sub-threshold topological FET devices (Invited Talk)
Start Time: 03:00 PM (30 Mins)
Speaker/Author: Prof. Bhaskaran Muralidharan, Department of Electrical Engineering, IIT Bombay
Presenter: Prof. Bhaskaran Muralidharan

Abstract: Using state-of-the-art quantum transport based device modeling, we propose novel "topo-tronic"device constructs - providing an effective route to channelize the tantalising possibilities offered by topological quantum

materials for emerging device design [1]. We propose a topological quantum field-effect transistor (TQFET) that be engineered to enable sub-thermionic transistor operation coupled with dissipationless ON-state conduction. Detailing the complex band translation physics related to the quantum spin Hall effect phase transition, It is the demonstrated transitions between the quantum spin-valley Hall (QSVH) and the spin quantum anomalous Hall (SQAH) phase can ultimately ensure the topological robustness of the ON state while surpassing the thermionic limit. We finally comment on other systems like superconducting hybrid systems that rely on Rashba spin-orbit coupling for advanced device functionalities and also a peek into our current ventures on understanding dephasing across topological channels [3].
References:
[1] K. Jana and B. Muralidharan, npj 2D Materials and Applications, 6, 19, (2022).
[2] S. Banerjee et.al., ArXiv: 2202.12044 (2022) (in revision at Phys Rev Applied).
[3] A. Basak, P. Brahma and B. Muralidharan, J. Phys D: Appl. Phys., 55, 075302, (2021).

9-3: Junction Less Ferroelectric FET on FDSOI for Non-Volatile Logic-In-Memory Applications (Oral)
Start Time: 03:30 PM (15 Mins)
Speaker/Author: Roopesh Singh (IIT BHU, India); Sumit Purkait (IIT BHU Varanasi, India); Shivam Verma (IIT BHU, Varanasi, India)
Presenter: Roopesh Singh

Abstract: Ferroelectricity in HZO-based thin films and its integration of ferroelectric field effect transistors (FeFET) into standard CMOS platforms has germinated new prospects in the field of non-volatile memory and non-volatile computing. The FeFET has emerged from a theoretical concept to many experimental demonstrations in recent years. FeFETs can be widely used in a variety of fields, including non-volatile memory, neuromorphic computing, logic-in-memory (LiM), and others. This paper proposes a novel silicon-on-insulator (SOI) based junction-less ferroelectric field effect transistor (JLFeFET). Further, an investigation of a non-volatile latch for non-volatile logic-in memory computing is also done using the proposed JLFeFET. The proposed JLFeFET offers huge possibilities for the design of low-power and high-speed non-volatile logic-in-memory applications. Using the TCAD simulations, JLFeFET of 20 nm HfO2 thickness has been demonstrated that achieves a memory window (MW) of 0.34 V. The fabrication flow is also proposed with an easy integration of the JLFeFET device in silicon-on-insulator (SOI) process. Further, the proposed non-volatile latch with JLFeFET displays significantly low power with respect to its non-volatile counterpart implemented using magnetic tunnel junction (MTJ) devices.

9-4: Ultra-low-power steep-slope transistors based on laterally confined monolayer MoSi2N4 (Invited Talk)
Start Time: 03:45 PM (30 Mins)
Speaker/Author: Prof. Amit Agarwal, IIT Kanpur, India
Presenter: Prof. Amit Agarwal

Abstract: Leakage current in transistors has become a critical limiting factor for realizing ultra-low-power transistors. The dominant part of the leakage current arises from the long tail of the thermally excited carriers of high energy. We solve this problem by using narrow bandwidth semiconductors which limits the thermionic leakage current by filtering out the high energy carriers. We demon- strate this by using laterally confined and passivated monolayer MoSi2N4 as a channel material in two-dimensional transistors. With this solution, the subthreshold slope can be reduced to remark- ably low values of up to ~ 20 mV/decade, compared to the thermally limited value of 60 mv/decade in conventional transistors at room temperature. We show that the unique electronic properties of narrow bandwidth conduction and valance bands is also shared by several other materials in the same series. This opens up new avenues for effectively tackling the OFF state current leakage and power dissipation problem and realizing ultra-low-power transistors.

Session No: 10 | Session Title: THz sensing and Imaging

Audi: 10 | 02:30 PM-04:15 PM | **Session Chair:** Dr. S. S. Prabhu
Track: RF, Millimeter and THz Technologies, Circuits and Systems (RF-THz)
Date: 12-Dec-22

10-1: SiGe/CMOS Technologies for Ku/Ka band SATCOM (Invited Talk)
Start Time: 02:30 PM (30 Mins)
Speaker/Author: Dr. Venkata Vanukuru, GlobalFoundries
Presenter: Dr. Venkata Vanukuru

Abstract: The concept of delivering internet connectivity from space is gaining widespread attention. This talk aims to cover various challenges at system, circuit, device and technology level in implementing ground terminals of SATCOM.

10-2: THz-driven strong-field lightwave electronics and nanoscale THz imaging (Invited Talk)
Start Time: 03:00 PM (30 Mins)
Speaker/Author: Prof. Peter Uhd Jepsen, Department of Electrical and Photonics Engineering, Technical UNiversity of Denmark
Presenter: Prof. Peter Uhd Jepsen

Abstract: Terahertz (THz) spectroscopy has been used for decades as a driver for the development of novel applications in sensing, nondestructive testing, and quality control. In the recent few years there has been an increased interest in using strong THz field for technologies that are close to fundamental research, but still is close to commercial use. I will discuss our recent development of the world's first THz-sensitive photomultiplier, THz-based imaging techniques for large-scale mapping of thin-film conductivity with focus on graphene in the semiconductor industry, and finally show the route towards mapping of thin-film conductivity with a resolution of 20 nanometers, using THz waves.

10-3: Wideband Linear-Circular and Linear-Cross Angular Stable THz Reflective Polarizer With Circular Ring Based Frequency Selective Surface (Oral)
Start Time: 03:30 PM (15 Mins)
Speaker/Author: Mohammad Abdul Shukoor (Indian Institute of Technology Palakkad, India); Tejas Shibu Bini and Nissan Kunju (TKM College of Engineering, India); Sukomal Dey (Indian Institute of Technology Palakkad, India)
Presenter: Mohammad Abdul Shukoor

Abstract: A novel multiband dual-polarized reflective polarizer is demonstrated in this article, which performs dual-operation like linear-cross and linear-circular conversions in the THz regime. The unitcell consists of a thin gold film coated modified circular rings-based Frequency Selective Surface (FSS) on top of a polyamide substrate grounded with a gold film to make the reflective design. Under normal incidence, the design performs the linear-cross conversion from 0.62-0.65 THz, 0.98-1.10 THz, and 1.74-1.80 THz, with a 90% minimum Polarization Conversion Ratio (PCR), respectively. In addition, it also demonstrates linear to circular conversion with Axial Ratio (≤ 3dB) from 0.58-0.59 THz, 0.69-0.90 THz, 1.18-1.67 THz, and 1.87-1.90THz. Multiple plasmonic resonances are the reason behind these conversions, which are visualized with surface current distribution analysis. The device performance is stable for Transverse Electric (TE) and Transverse Magnetic (TM) incidences up to 45 o . The proposed converter's dual-polarized linear-cross and linear-circular conversion influence real-time THz applications significantly.

10-4: Ultrafast Spintronic THz Emitters (Invited Talk - Withdrawn)
Start Time: 03:45 PM (30 Mins)
Speaker/Author: Prof. Sunil Kumar, Indian Institute of Technology Delhi
Presenter: Prof. Sunil Kumar

Abstract: Femtosecond laser excited spintronic heterostructures have emerged as a potential candidate for powerful and broadband THz radiation sources. Increasingly popular systems in this regard are the bi- and tri-layer combinations of thin films of ferromagnetic (FM) metal and nonmagnetic (NM) heavy metal. Inverse spin Hall effect (ISHE) in the NM layer is majorly considered as the main mechanism to develop a transient current source which emits THz radiation. Towards optimizing the optical to THz conversion efficiency and broadband gapless THz spectrum from these THz emitters, the optical ultrafast pulse characteristics, the FM and NM material types and their optimal thickness are the key control parameters. Some of these will be discussed in this talk through presentation of a few of the recent results from our group at IIT Delhi.

Session No: 11 | Session Title: Design Technology Co-Optimization
Audi: 11 | 02:30 PM-04:30 PM | **Session Chair:** Dr. Arun Joseph
Track: Advanced Logic Technologies (ALT)
Date: 12-Dec-22

11-1: The Requirements and Innovations for Process Window Discovery (Invited Talk)
Start Time: 02:30 PM (30 Mins)
Speaker/Author: Mr. Chen, Li (Hardy), KLA

Presenter: Mr. Chen, Li

Abstract: Process Window Discovery and Qualification is the foundation of every new technology node where different process variables are tested and characterized in search for the best combined approach. Aggressively scaled CD sizes and the use of EUV scanners have made the work of PWD even more demanding and challenging. The talk is going to walk through some key steps in process window discovery along with their requirements and innovations.

11-2: DTCO: How the industry has evolved (Invited Talk)
Start Time: 03:00 PM (30 Mins)
Speaker/Author: Mr. Rwik Sengupta, Cadence, United States
Presenter: Mr. Rwik Sengupta

Abstract: Since 1965, when Gordon Moore made his now famous self-fulfilling prophecy, optical scaling and material systems enabled a direct 0.5x area scaling node over node, for the next 30 years or so. While in no way was this scaling straightforward i.e.: engineering Innovation was needed; We were not approaching physical limits of material systems or optical limits of the printing systems. As area scaled, device and parasitic capacitance scaled almost linearly, without appreciable increase in effective Resistance or Leakage currents. This fulfilled the conditions for Dennard's Law, enabling a geometric shrink driven performance boost and power reduction. In the early 2000s, for the 32/28mm node the rules of engagement changed, driven primarily by increase in leakage. However, design was still somewhat isolated from the disruption by clever technology decisions. By the time the industry was developing the 22/16nm nodes in 2005, it was no longer possible to optimize technology alone due to limits of optical/patterning systems, and the term DTCO was coined. Since then, DTCO has evolved to design around patterning and integration challenges, determine device and interconnect choices to drive PPA as we push the physical electrical limits of semiconductor manufacturing. My talk will cover some interesting aspects of how DTCO has impacted Technology Definition since its conception in 2005 to current day.

11-3: DTCO for Advanced Technology Device and Circuit Designs (Invited Talk)
Start Time: 03:30 PM (30 Mins)
Speaker/Author: Dr. Vinay Kumar Dasarapu, Synopsys India Pvt Ltd
Presenter: Dr. Vinay Kumar Dasarapu

Abstract: For sub-10 nm technology nodes, the pitch scaling began to slow down, and it is expected to cease as it reaches 1 nm node. To keep the pace of transistor density increments at 45% density increase per node, industry is employing sophisticated Design-Technology Co- Optimization (DTCO) methodologies. Gate All Around FETs (GAAFETs) have been introduced as an advanced to the FinFET architectures, with specific advantages of GAAFETs over FinFETs: i) increased gate control by having the gate all around the channel, and ii) higher transistor density by utilizing the vertical structure with multiple channel regions per fin. In this work, we will analyze the quantum confinement effects due to small cross section of GAAFET channels on the device gate capacitance. To achieve the best possible Power-Performance-Area (PPA) trade-off of logic circuits, need to optimize the 3-D structure of the device for reduced parasitic components. A comprehensive optimization DTCO methodology is required to achieve the target results.

11-4: CMOS scaling: From Design into System Technology Co-Optimization (Invited Talk)
Start Time: 04:00 PM (30 Mins)
Speaker/Author: Dr. Julien Ryckaert, imec, Belgium
Presenter: Dr. Julien Ryckaert

Abstract: Scaling is driven by the perspective of more function per unit cost. This paradigm has essentially been fueled with increasing transistor density by building ever more compact devices and finer interconnect capabilities. We are approaching records in feature sizes that starts questioning its viability moving forward. The entire Mendeleev table has been screened and manufacturing machines reach extreme levels in precision. However, an SoC is not composed of a monolithic set of functions, from compute blocks to memorization very different functions are expected from CMOS devices, not to mention the whole infrastructure that wraps the system (power and clock distribution, short signal nets and long signal nets, IOs and PLLs,...). The SoC is a vastly heterogeneous system. In order to keep scaling system performance, technology will not need to embrace that heterogeneity and find ways to leverage unique technology capabilities that improve system performance. This can only go hand in hand with a revision of system design practices and introducing novel architectures. CMOS Scaling is entering the era of System-Technology Co-Optimization. We will be talking about concepts leaning in

that direction, such as backside processing and bonding technologies for smart partitioning, and extrapolate to the broader vision of the CMOS heterogeneous platform: CMOS 2.0.

Session No: 12 | Session Title: 2D materials for photonics and optoelectronic
Audi: 1 | 04:15 PM-06:00 PM | **Session Chair:** Prof. Mario Lanza
Track: 2D Material Based Technologies (2DT)
Date: 12-Dec-22

12-1: 2D Materials for Emerging Photonics (Invited Talk)
Start Time: 04:15 PM (30 Mins)
Speaker/Author: Prof. Zhipei Sun, Aalto University
Presenter: Prof. Zhipei Sun

Abstract: Photonics is of great significance for various emerging and future applications, such as data interconnection, sensing, imaging and information processing. Here, I will present our recent results on engineering two-dimensional layered materials and their heterostructures for various photonic and optoelectronic applications, such as light sources, modulators, sensors, and detectors. I will also introduce our new advances in hybrid structures, such as mixed-dimensional heterostructures, plasmonic structures, and silicon/fibre waveguides integrated structures, to address the challenges of emerging photonics.

12-2: Quantum emitters in 2D materials (Invited Talk)
Start Time: 04:45 PM (30 Mins)
Speaker/Author: Dr. Biswanath Chakraborty, Indian Institute of Technology Jammu
Presenter: Dr. Biswanath Chakraborty

Abstract: Developing quantum emitters in a deterministic way to address future quantum information technologies has propelled intense activities in the recent past. Various studies on a wide variety of materials have been conducted to find out ideal sources of a robust and high-purity single photon. Atomically thin van der Waals materials with unique properties have been explored for developing single photon emitters that can even be integrated with photonic platforms.
Here we discuss the generation and characterization of such quantum emitters operating at room temperature. We perform time correlation measurements to establish single-photon properties.

12-3: Edge-Epitaxial Growth of MoS2-WS2 Lateral Heterostructure and Their Optoelectronic Properties (Oral)
Start Time: 05:15 PM (15 Mins)
Speaker/Author: Biswajeet Nayak, Suman Kumar Chakraborty and Rajdeep Banerjee (Indian Institute of Technology Kharagpur, India); Purbasha Ray (Indian Institute of Technology, Kharagpur, India); Baisali Kundu (Indian Institute of Technology Kharagpur, India); Sagar Bisoyi (Kalinga Institute of Industrial Technology Bhubaneswar, India); Rabaya Basori (Indian Institute of Technology Kharagpur, India); Gopal K Pradhan (Kalinga Institute of Industrial Technology Bhubaneswar, India); Dipak Kumar Goswami (IIT KHARAGPUR, India); Prasana Kumar Sahoo (Indian Institute of Technology Kharagpur, India)
Presenter: Biswajeet Nayak, Suman Kumar Chakraborty and Rajdeep Banerjee (Indian Institute of Technology Kharagpur, India); Purbasha Ray (Indian Institute of Technology, Kharagpur, India); Baisali Kundu (Indian Institute of Technology Kharagpur, India); Sagar Bisoyi (Kalinga Institute of Industrial Technology Bhubaneswar, India); Rabaya Basori (Indian Institute of Technology Kharagpur, India); Gopal K Pradhan (Kalinga Institute of Industrial Technology Bhubaneswar, India); Dipak Kumar Goswami (IIT KHARAGPUR, India); Prasana Kumar Sahoo (Indian Institute of Technology Kharagpur, India)

Abstract: We reported the direct growth of electronic grade 2D MoS2-WS2 lateral heterostructures (LHS) by controlling critical physicochemical parameters using a water-assisted chemical vapor deposition technique. Raman and photoluminescence spectroscopy and transport measurements were used to standardize their optical and electronic characteristics. In addition, the role of metal contacts in the transport characteristics in the field-effect transistor geometry of the LHS was evaluated.

12-4: Utilizing Quantum Geometry and Topology for Enabling Integrated Chiral Photonics (Invited Talk)
Start Time: 05:30 PM (30 Mins)
Speaker/Author: Prof. Ritesh Agarwal, University of Pennsylvania
Presenter: Prof. Ritesh Agarwal

Abstract: Classical and quantum computing devices need to ferry vast amounts of data and optical interconnects provide a promising approach allowing faster speeds and larger bandwidths. Critical interconnect components are

light sources, waveguides and detectors. Currently, the information is encoded in intensity and frequency but other degrees of freedom (DOFs) such as photon-spin and spatial orbital angular momentum modes (OAM) should be utilized to enhance the capacity of optical links. Therefore, new materials and devices that can produce, transmit and detect light with complex polarization and spatial modes are needed. We will discuss recent developments towards the development of on-chip lasers, waveguides and photodetectors that are sensitive to photon spin and OAM modes that can enable the development of integrated chiral photonic systems.

Session No: 13 | Session Title: Compact Modelling, PDK and BiCMOS Process
Audi: 2 | 04:15 PM-06:00 PM | **Session Chair:** Prof. Avirup Dasgupta
Track: Modelling and Simulations (MS)
Date: 12-Dec-22

13-1: PDK Development - Philosophy and Best Practices (Invited Talk)
Start Time: 04:15 PM (30 Mins)
Speaker/Author: Mr. Somu Ghosh, Texas Instruments, India
Presenter: Mr. Somu Ghosh

Abstract: In an enterprise environment, designers consume and build on technology information using the Process Development Kit (PDK). In this tutorial we will cover the PDK development flow, consumables that go into the PDK and philosophy and design practices that are associated with building the PDK. This tutorial will give an umbrella view of the PDK and unique aspects of building PDK for different technologies.

13-2: Extraction of Output Conductance Parameters From Simple DC IV Measurements for a Compact Model (Oral)
Start Time: 04:45 PM (15 Mins)
Speaker/Author: Sreenidhi Turuvekere (GlobalFoundries Engineering Pvt. Ltd., India); Anamika Singh Pratiyush (Global Foundries Engineering Pvt. Ltd. India, India); Srikanth Srihari (GLOBALFOUNDRIES, India); Ananth Sundaram (Globalfoundries Engineering Private Limited, India)
Presenter: Sreenidhi Turuvekere

Abstract: A method to extract channel length modulation (CLM) and drain induced barrier lowering (DIBL) parameters from simple output characteristics is presented. The extracted DIBL and CLM parameters provide insights while setting compact model parameters, thereby easing the model extraction flow. This method is validated against DC and RF hardware data.

13-3: An Indigenous Low-Cost Robust BiCMOS Process Flow for NavIC Applications (Oral)
Start Time: 05:00 PM (15 Mins)
Speaker/Author: Om Maheshwari and Ravins Katiyar (Indian Institute of Technology Gandhinagar, India); Amitava DasGupta (Indian Institute of Technology Madras, India); Anjan Chakravorty (IIT Madras, India); Deleep Nair (Indian Institute of Technology Madras, India); Nihar Ranjan Mohapatra (IIT Gandhinagar, India)
Presenter: Om Maheshwari and Ravins Katiyar

Abstract: A low-cost BiCMOS process integrable with Semi-Conductor Laboratory's (SCL's) 180 nm CMOS process flow is developed for designing indigenous application-specific integrated circuits (ASICs) for Indian regional satellite navigation system NavIC. The process is optimized for realizing high frequency (HF) as well as high voltage (HV) double polysilicon bipolar junction transistors and is robust to process variations. The designed HF device has fT/fmax ~ 29/50 GHz, and the HV device has a breakdown voltage of ~ 10 V.
13-4: Improved Surface Potential Based Compact Model for Bulk MOSFETs at Cryogenic Temperatures (Oral)
Start Time: 05:15 PM (15 Mins)
Speaker/Author: Wajid Manzoor (Indian Institute of Technology Kanpur, India); Ravi Goel (IIT Kanpur, India); Aloke Dutta (IITK, India); Yogesh Chauhan (Indian Institute Of Technology, India)
Presenter: Wajid Manzoor (Indian Institute of Technology Kanpur, India); Ravi Goel (IIT Kanpur, India); Aloke Dutta (IITK, India); Yogesh Chauhan (Indian Institute Of Technology, India)

Abstract: In this article, we present an improved surface potential-based compact model for calculating the characteristics of bulk MOSFETs at cryogenic temperatures. The existing PSP model calculates the surface potential using the analytical solution of a transcendental equation derived under the assumption of complete ionization of the dopants. However, this assumption is invalid at cryogenic temperatures because of the effect of dopant freeze-out. Therefore, a transcendental equation, including temperature-related physical effects, is used in this work to obtain an analytical solution of the surface potential for the PSP model, valid from room temperature

all the way down to cryogenic temperatures. The improved PSP model is validated by matching its results for the drain current with experimental data, and those for the gate capacitances with TCAD simulations.
13-5: IIT Madras Charge Based Compact Model (ICM) for GaN based HEMTs (Invited Talk)
Start Time: 05:30 PM (30 Mins)
Speaker/Author: Prof. Amitava DasGupta, IIT Madras, India
Presenter: Prof. Amitava DasGupta

Abstract: A computationally efficient compact model of GaN-based HEMTs suitable for DC, small signal as well as transient simulations is presented.
At first, a unified expression for 2DEG charge density is formulated. Considering drift-diffusion model and charge linearization in the channel, an expression for the drain current is derived in terms of the electron charge densities at the source and drain ends. Other effects such as DIBL, CLM, vertical field dependence on mobility and self-heating are incorporated. The access regions are modelled using additional HEMTs similar to the intrinsic transistor. A model for gate-to-source and gate-to-drain currents is derived in terms of the terminal charges, which are obtained using Ward-Dutton charge partitioning scheme. The model includes the effect of buffer traps and is able to capture the dynamic behaviour of HEMTs and current collapse.
The model equations are implemented in Verilog-A and validated by comparison with experimental data for a wide range devices and under different operating conditions.

Session No: 14 | Session Title: State of the art Ga2O3 Devices & Physics
Audi: 3 | 04:15 PM-06:00 PM | **Session Chair:** Prof. Srabanti Chowdhury (Stanford)
Track: Wide Bandgap Power Semiconductor Technologies (WPSD)
Date: 12-Dec-22

14-1: Ultrawide Bandgap β-Ga2O3 Transistors for Efficient Multi-Kilovolt Power Switching (Invited Paper)
Start Time: 04:15 PM (30 Mins)
Speaker/Author: Arkka Bhattacharyya, Saurav Roy and Carl Peterson (University of California Santa Barbara, USA); Fikadu Alema and Andrei Osinsky (Agnitron Technology Inc, USA); Sriram Krishnamoorthy (University of California Santa Barbara, USA)
Presenter: Arkka Bhattacharyya

Abstract: β-Ga2O3 has emerged as a material that demonstrates numerous strengths for next-generation high voltage/power applications. Its projected material power figure of merit (PFOM) is almost 3500×, 10×, and 4× higher than that of Silicon, SiC, and bulk GaN. In this work, state-of-the-art electron mobilities, contact resistance values, breakdown voltages, and power figures of merit are demonstrated in β-Ga2O3 epitaxial films and power devices. Record low specific contact resistance (ϱc) and total contact resistance (RC) of 1.62 × 10 −7 Ω.cm 2 and 0.023 Ω.mm were realized for β-Ga2O3: Si films
with n > 3 × 10 20 cm −3 . A low-temperature un-doped buffer-channel stack design is developed, which demonstrates record high Hall (up to 196 cm 2 /Vs) and drift electron mobilities (up to 125 cm 2 /Vs) in doped β-Ga2O3 channels allowing for low ON resistances (RON) in β-Ga2O3 MESFETs with record high PFOM close to ~ 1GW/cm 2 . 4.4 kV class β-Ga2O3 lateral MESFETs surpassing theoretical UFOM of Silicon are also realized.

14-2: β-Ga2O3 Dielectric Superjunction Schottky Barrier Diode Exceeding SiC Unipolar Figure of Merit: A Novel Approach to Realizing Superjunction Devices Without p-Type Doping (Oral)
Start Time: 04:45 PM (15 Mins)
Speaker/Author: Saurav Roy, Arkka Bhattacharyya, Carl Peterson and Sriram Krishnamoorthy (University of California Santa Barbara, USA)
Presenter: Saurav Roy

Abstract: We demonstrate lateral β-Ga2O3 Schottky barrier diode (SBD) with a high permittivity (high-k) dielectric superjunction (SJ) structure. Extreme permittivity dielectric (BaTiO3) with dielectric constant of 220 is used to uniformly distribute the electric field in a MOVPE-grown lateral drift layer, which circumvents the extreme difficulties in achieving charge balance using conventional p-n superjunction structures in β-Ga2O3 due to the lack of shallow acceptors. SBD on an epilayer with a sheet charge of 1.5×10 13 cm -2 demonstrates a specific on resistance (Ron-sp) of 0.83 mΩ-cm -2 and a breakdown voltage VBR of 1487 V for an anode to cathode length of 5 microns, rendering a Power figure of Merit (PFOM) of-2.7 GW/cm -2 when normalized to the active current conducting area. These results using the proposed device structure demonstrates the promise of β-Ga2O3-based devices in multi-kilovolt class applications.

14-3: Demonstration of Ga2O3 Trigate Transistors on (100) Silicon Substrates (Oral)
Start Time: 05:00 PM (15 Mins)
Speaker/Author: Saravanan Yuvaraja, Vishal Khandelwal, Shibin Krishna, Yi Lu, Zhiyuan Liu, Mritunjay Kumar, Dhanu Chettri, Xiao Tang and Glen Isaac Maciel García (King Abdullah University of Science and Technology, Saudi Arabia); Che-Hao Liao and Xiaohang Li (KAUST, Saudi Arabia)
Presenter: Saravanan Yuvaraja

Abstract: In this paper we demonstrated the UWBG Ga2O3 trigate transistors heterogeneously integrated on silicon substrate. This trigate transistor operates in depletion mode having decent Ion/Ioff ratio (10 5) and high transconductance (1 μS). Followed by the mobility is around 1.2 cm 2 /V. s. This work suggests that the ultrawide bandgap oxide transistors can be fabricated on various heterogenous substrates to achieve highly integrated, low cost, and robust electronics.

14-4: Gate Stack Engineering in n-Type (-201) β-Ga2O3 Transistors (Oral)
Start Time: 05:15 PM (15 Mins)
Speaker/Author: Vishal Khandelwal and Saravanan Yuvaraja (King Abdullah University of Science and Technology, Saudi Arabia); Chuanju Wang (King Abdullah University of Science and Technology Saudi Arabia, Saudi Arabia); Dhanu Chettri (King Abdullah University of Science and Technology, Saudi Arabia); Xiaohang Li (KAUST, Saudi Arabia)
Presenter: Vishal Khandelwal

Abstract: A systematic study of Al2O3 and SiO2/Al2O3 dielectric on β-Ga2O3 is carried out including the effect of the forming gas annealing. Capacitance-voltage (C-V) curve of the Al2O3/Ga2O3 gate stack shows a large hysteresis and sweep-to-sweep C-V shift compared to SiO2/Al2O3/Ga2O3 case, which suggests SiO2 interlayer reduces the defect density in Al2O3/Ga2O3 gate stack. In addition, forming gas annealing further suppresses the interface and border traps density in both Al2O3/Ga2O3 and SiO2/Al2O3/Ga2O3 gate stacks. A thin film transistor (TFT) with annealed SiO2/Al2O3 dielectric has an on-off ratio of ~106, a subthreshold swing (SS) of ~ 0.75 V/decade, and a hysteresis width (VHy) of ~ 0.5 V compared to an on-off ratio of ~105, a SS of ~1.2 V/decade, and a VHy of ~2 V in the controlled TFT with unannealed Al2O3 dielectric. The increased on-off ratio by one order, reduced SS by > 400 mV/decade, and VHy by >1.5 V is attributed to decreased interface and border traps in annealed SiO2/Al2O3 compared to unannealed Al2O3/Ga2O3 gate stack. Interface trap density is calculated by VHy of the transistor, which showed a five-time reduction in annealed SiO2/Al2O3/Ga2O3 compared to the unannealed Al2O3/Ga2O3 gate stack. This study suggests that annealed SiO2/Al2O3 dielectric stack is promising for β-Ga2O3 transistors.

14-5: Investigation and Comparison of Deep Acceptors in β-Ga2O3 using Defect Spectroscopies (Invited Talk)
Start Time: 05:30 PM (30 Mins)
Speaker/Author: Prof. Steven Ringel, The Ohio State University
Presenter: Prof. Steven Ringel

Abstract: Beta phase gallium oxide (β-Ga2O3) is a strong contender for next-generation high voltage and RF device applications. A key component of such devices is a semi-insulating, highly resistive buffer layer or substrate. To date, iron (Fe) has been the preferred acceptor impurity to achieve semi-insulating β-Ga2O3. Iron produces an energy level at EC-0.8 eV, which has been substantiated by theoretical and experimental studies and enables highly resistive material. However, it has also been shown that residual Fe impurities can result in device switching instabilities since the Fermi level can modulate the occupancy of the Fe trap state during standard biasing conditions. While progress to mitigate the impact of residual Fe impurities has occurred, there is also interest in exploring acceptors with much deeper energy levels to avoid device instabilities. Magnesium (Mg) and nitrogen (N) have emerged as candidates based on their predicted energy levels of EC-3.3 eV and EC-2.8 eV, respectively (H. Peelaers, et al., APL Mater. 7, 022519, 2019). This presentation will compare each acceptor, with a primary focus on N, using deep level optical spectroscopy (DLOS) and thermally based deep level transient spectroscopy (DLTS). Here, N acceptors were introduced into HVPE-grown β-Ga2O3 by ion implantation. A uniform N-implantation profile was used targeting multiple doses in different samples, followed by an activation anneal. DLTS and DLOS measurements were applied before and after annealing. After implantation, multiple trap states appeared, most of which were removed by annealing, leaving a single, new state at EC-2.9 eV, with a Frank-Condon energy of 1.4 eV. The concentration of this state monotonically tracked with nitrogen concentration from SIMS. This energy level closely matches predicted values for an acceptor-like defect due to nitrogen atoms occupying the oxygen III sites, determined by density functional theory (DFT) calculations (H. Peelaers, et al., APL Mater. 7, 022519, 2019; Y.K. Frodason, et al. J. Appl. Phys. 127, 075701, 2020), The much deeper energy

compared with Fe could imply a significantly lower operational instability than the shallower Fe acceptor at EC-0.8 eV. However, we found that the below midgap position of the NO(III) level, coupled with its small optical cross-section, complicates the trap concentration analysis by DLOS, which is important for understanding how to characterize very deep states in β-Ga2O3. Simultaneous hole emission to the valence band and electron emission to the conduction band was seen. Similar challenges might be present for Mg doping as well. The impact of this behavior on DLOS analysis is discussed, and a method to resolve this complication will be presented, which is needed to guide further optimization of this critical step in gallium oxide device development.

Session No: 15 | Session Title: Advanced Sensing
Audi: 4 | 04:30 PM-06:00 PM | **Session Chair:** Dr. Kiran Aatre
Track: Sensors and Bio-Electronics (SBE)
Date: 12-Dec-22

15-1: Hydrogel based sensors for medical diagnostic applications (Invited Talk)
Start Time: 04:30 PM (30 Mins)
Speaker/Author: Dr. Dhananjaya Dendukuri, Achira Labs
Presenter: Dr. Dhananjaya Dendukuri

Abstract: Synthetically fabricated hydrogel particles are increasingly used for bio sensing applications. Newly developed techniques allow fabrication of hydrogels with different morphologies, spatially segregated functionalization and tuned material properties. Hydrogel sensors embedded inside microfluidic devices have a number of advantages including multiplexing, good stability and low non-specific binding. The talk will discuss hydrogel sensor capabilities on Achira's point-of-care platform.

15-2: Design and Synthesis of a Polymer for Cr(III) Ions Sensing (Oral)
Start Time: 05:00 PM (15 Mins)
Speaker/Author: Aman Thakur, Vishakha Chauhan and Praveen C Ramamurthy (Indian Institute of Science, India)
Presenter: Aman Thakur

Abstract: A fluorene and amino-based conjugated polymer (PFluDNH2) was designed to selectively detect chromium (III) ions. The synthesis of the sensing polymer molecules was achieved in four steps which involved the formation of a diamino intermediate and the polymerization of this intermediate with a fluorene derivative. The structural elucidation of the synthesized molecules was performed using FTIR, 1H-NMR, 13C-NMR, and UV-Vis spectroscopic techniques. The cyclic-voltammetric experiments were performed to examine the electrochemical properties. Optical properties were studied by the photoluminescence (PL) technique. Synthesized PFluDNH2 displayed enhancement in fluorescence intensity upon selectively interacting with Cr (III) ions by showing chelation-enhanced fluorescent (CHEF) effect. The intensity increased after an excitation wavelength of 350 nm. The synthesized polymer showed good potential for metal ion detection and light-emitting devices.

15-3: Optical Imaging of Up-Conversion Nanoparticles Attached Magnetic Nano-Swimmers Through Tissue-Mimicking Phantoms (Oral)
Start Time: 05:15 PM (15 Mins)
Speaker/Author: Ankur Jaiswar, Tanmoyendu Chakraborty, Brateen Pal and Ambarish Ghosh (Indian Institute of Science, India)
Presenter: Ankur Jaiswar

Abstract: Biological tissues have optical scattering and absorption properties, making them appear opaque. Therefore, visualizing the deep intact tissue is one of the major challenges in Biomedical imaging. Optical imaging using the Near-infrared source provides an advantage of high-resolution deep tissue imaging but has the limitation of autofluorescence and scattering. Lanthanide-doped Up-conversion nanoparticles (UPCNs) are the new generation fluorophores that show a unique luminescence property and attract greater attention in biomedical imaging. In this work, we have attached the UPCNs to the magnetic helical nano-swimmers to be used as NIR probe and optically imaged them through the tissue-mimicking phantoms.

15-4: MoS2 nanoflowers decorated e-textile for Ammonia sensing applications (Oral)
Start Time: 05:30 PM (15 Mins)
Speaker/Author: Sushmitha Veeralingam (Indian Institute of Technology Hyderabad, India); Sushmee Badhulika (IIT Hyderabad, India)

Presenter: Sushmitha Veeralingam
Abstract: For NH3 sensing applications, power efficiency and excellent sensitivity are particularly desirable. Titanium (Ti) functionalized Molybdenum Disulfide (MoS2) interspersed polypropylene (PP) cloth has been used for ammonia gas sensor applications. XRD spectroscopy confirms the formation of trigonal phase Ti@MoS2 while Raman spectroscopy reveals the few-layered structure of Ti@MoS2 nanoflowers. Morphological characterization studies reveal the deposition of Ti@MoS2 nanoflowers over the PP cloth. The Ti- MoS2 on PP cloth-based gas sensor displays an excellent response with a wide dynamic sensing range of ammonia gas from 200 ppb - 2600 ppb at room temperature, with high sensitivity, selectivity and a rapid response time of 50 s. This study explores the e-textile-based ammonia gas sensor fabricated with excellent potential for health diagnostic applications.

15-5: Chemical Synthesis and Application of Silver Decorated Reduced Graphene as an Economically Viable Surface Enhanced Raman Scattering Based Substrate for Detection of Analytes in Trace Quantities (Oral)
Start Time: 05:45 PM (15 Mins)
Speaker/Author: Sibashish Chakraborty, Vimarsh Awasthi and Richa Goel (Indian Institute of Technology Delhi India, India); Satish Dubey (IIT Delhi, India)
Presenter: Sibashish Chakraborty

Abstract: In this work, we present a simple, economically viable technique of chemically synthesizing silver-decorated reduced graphene (Ag-rG) and its application in SERS analyte detection. We detected R6G (20 μL) up to 10-6 M using Ag-rG as a SERS-active substrate. R6G, a dye, is irradiated by a laser source (λ =785nm) and Raman spectra are acquired using integrated Raman setup (Renishaw). Ag-rG can be used for in-situ explosive detection, food/water adulterant detection, bio-diagnostics, narco-analysis, etc.

Session No: 16 | Session Title: Materials and Device Application Approaches

Audi: 5 | 04:30 PM-06:00 PM | **Session Chair:** Prof. Subho Dasgupta
Track: Macroelectronics & Displays: Devices, Circuits & Systems (DIS)
Date: 12-Dec-22

16-1: Strain Insensitive Thin Film Transistor Circuits (Invited Talk)
Start Time: 04:30 PM (30 Mins)
Speaker/Author: Prof. Sanjiv Sambandan, Indian Institute of Science, India
Presenter: Prof. Sanjiv Sambandan

Abstract: Thin film transistors (TFT) promise high density integrated circuits and systems on diverse substrates such as glass, plastics and textiles. Recent years have seen a growing interest in the development of integrated systems that can both bend and stretch. These circuits are developed on elastomeric substrates that have a relatively low modulus of elasticity.
However, such requirements pose interesting questions related to the design of TFT circuits on these substrates. If there is positive strain along the source-drain direction, it is known that the threshold voltage reduces, and mobility increases in metal oxide TFTs. Based on this understanding, the question one can ask is – can we design TFT circuits whose transfer function remains strain independent? Here I discuss some key ideas that may enable the design of such circuits.

16-2: Acoustoelectric Current in Poly(3-Hexylthiophene) (Oral)
Start Time: 05:00 PM (15 Mins)
Speaker/Author: Paromita Bhattacharjee (Mems & Nems Lab, Centre for Nanotechnology & IIT Guwahati, India); Parameswar Krishnan Iyer (Indian Institute of Technology Guwahati, India); Harshal B. Nemade (Indian Institute of Technology Guwahati)
Presenter: Paromita Bhattacharjee

Abstract: The paper demonstrates frequency dependence of acoustoelectric current generated in thin film of an organic semiconductor, regioregular poly(3-hexylthiophene) spin coated on surface acoustic wave (SAW) devices. The acoustoelectric (AE) effect assists in the hopping of charges by transfer of wave momentum and energy, and increases current in presence of SAW. The current was observed to enhance dominantly at the resonance frequency of the device, while it was also observed to spread around the resonance frequency attributed to maximum wave energy transfer at resonance and nominal transfer at other frequencies. The AE effect was independently studied in different piezoelectric substrates generating Shear horizontal and Rayleigh SAW, in order to verify the observed phenomenon.

16-3: Design of Bi-Layered Strong Microwave Absorber Based on Polymer-Fly Ash Cenosphere Composite With a Data-Driven Approach (Oral)
Start Time: 05:15 PM (15 Mins)
Speaker/Author: Pritom Bora (Indian Institute of Science & ICER, India); Bibhusita Mahanta, Kishore K and Praveen C Ramamurthy (Indian Institute of Science, India)
Presenter: Pritom Bora

Abstract: In this work, a strong microwave absorption characteristic viz., minimum reflection loss (RL) -69.5 dB (8.2-12.4 GHz absorption bandwidth i.e., RL≤ -10 dB) is evaluated for the bi-layered polyvinyl butyral (PVB)-polyaniline (PANI) coated fly ash cenosphere (FAC) composite. Materials data-driven approach is used to model and optimize the associated parameters (based on an experimental evaluation), and hence to realize the best RL. The outstanding RL performance is achieved for the 10 wt% PANI-FAC loaded PVB (top layer, thickness 1.5 mm) and 6 wt% PANI-FAC loaded PVB (a bottom layer, thickness 2 mm).

16-4: Advanced optoelectronic platform technologies for neuroengineering and robotics (Invited Talk)
Start Time: 05:30 PM (30 Mins)
Speaker/Author: Prof. Ajay Pandey, Queensland University of Technology, Brisbane, QLD, Australia
Presenter: Prof. Ajay Pandey

Abstract: Close loop and intelligent sensing systems with high specificity are vital to the progress of robotics and neuroscience. In neuroscience, we need neuro-engineering tools that can map ensemble of neurons in the brain with micron-resolution to understand the complexity associated with neuronal circuits, while on the other hand we need energy efficient and up-scalable technologies that can capture mechanical interactions between an object with the elegance of human skin for solving the physical manipulation challenge in robotics. In this talk, I will introduce prospects and examples of molecular optoelectronic systems that are suitably positioned to provide micro and macro level sensing. The suitability of this platform technology for optoegentics, proprioception and in form of robotic skin will be discussed.

Session No: 17 | Session Title: Photo-Rechargeable and High-Capacity Batteries

Audi: 6 | 04:15 PM-06:00 PM | **Session Chair:** Prof. Praveen Ramamurthy
Track: Energy Storage and Batteries (ESB)
Date: 12-Dec-22

17-1: Significance of Operando Investigations for Understanding the Electrochemical Mechanism of Battery Materials (Invited Talk)
Start Time: 04:15 PM (30 Mins)
Speaker/Author: Dr. Ditty Dixon, School of Chemical Sciences, Mahatma Gandhi University, Kottaym, India
Presenter: Dr. Ditty Dixon

Abstract: As far as electromobility is concerned, Li-ion battery (LIB) is at the forefront of current energy storage systems. In a LIB, positive electrode (cathode) is the capacity limiting and negative electrode (anode) is important for determining the safety. In this regard, several electrode materials (anode or cathode) are proposed or developed, those claim to exhibit superior performance in terms of efficiencies, rate capability, discharge capacity, etc. One of the key factors considered during development of novel electrode materials for battery technology is the cost and availability of the elements present. For e.g., Iron and Manganese may be preferred over Cobalt or Vanadium for novel materials as both Co and V are considered less abundant critical elements. Hence, more new materials are expected to be developed in the future and for this operando investigation is extremely important. The talk will give an overview of operando techniques used for investigating battery materials.

17-2: Role of exchange-correlation functionals in migration barrier predictions (Invited Talk)
Start Time: 04:45 PM (30 Mins)
Speaker/Author: Dr. Sai Gautam Gopalakrishnan, Indian Institute of Science, India
Presenter: Dr. Sai Gautam Gopalakrishnan

Abstract: A critical factor that influences the rate performance of batteries is the diffusion of the electroactive ions in the active materials, i.e., solid electrodes and/or electrolytes, which in turn is largely influenced by the ionic migration barriers (Em) within host frameworks. Determining Em precisely using experimental techniques, such as electrochemical impedance, variable temperature nuclear magnetic resonance, etc. is not a trivial task. Computationally, evaluating Em is often done via density functional theory (DFT)-based nudged elastic band (NEB) calculations or ab initio molecular dynamics (AIMD) simulations. Typically, DFT-NEB can yield a direct

estimate of Em in a given material, while AIMD relies on statistical sampling of migration events (which becomes more difficult with increasing Em values). Hence, DFT-NEB is the preferred computational choice to determine Em. However, the accuracy of DFT-NEB calculations in estimating Em is dependent on the choice of exchange-correlation (XC) functionals, and the errors associated with using different XC frameworks has not been accurately quantified yet. Hence, in the first part of my talk, I will focus on assessing the accuracy of different XC frameworks (versus experiments) in estimating Em in a wide variety of electrode and solid electrolyte materials. Importantly, we find that the strongly constrained and appropriately normed functional yields better accuracy of Em on average, albeit with significant convergence difficulties and notable exceptions of high inaccuracy, while the generalised gradient approximation provides robust qualitative trends in its Em predictions. I will also discuss about the role of uniform background charge and the climbing image approximation in Em predictions.

17-3: Rigidity Transition in Chalcogenide Glasses: Dynamic Nano-Indentation and Diffuse Reflectance Spectroscopic Studies (Oral)
Start Time: 05:15 PM (15 Mins)
Speaker/Author: Abhishek Chaturvedi (Indian Institute of Science, Bengaluru, India)
Presenter: Abhishek Chaturvedi

Abstract: Rigidity Transitions in quaternary glasses were investigated using dynamic nanoindentation and DRS reflectance spectroscopy in Ge 15Te 80-xIn 5Ag x glasses. In quasi-static properties such as reduced modulus, E r and hardness, H, an extended rigidity transition with distinct floppy, intermediate
and rigid phase is observed, while indentation toughness, K c and brittleness index, BI exhibits a rigidity transition at x =12. Floppy modes exhibit higher K c values when compared to rigid modes. Dynamic visco-elastic property, storage modulus vs frequency, f exhibits a trend reversal for floppy and rigid phases, which is attributed to difference in heat losses. The manifestation of intermediate phase (IP) in optical band gap (E g) is observed in the composition range ($8 \leq x \leq 14$) at. %.

17-4: High Energy and High Power Supercapacitors Using Nanocomposites for Consumer Electronics (Invited Talk)
Start Time: 05:30 PM (30 Mins)
Speaker/Author: Prof. Perumal Elumalai, Pondicherry University
Presenter: Prof. Perumal Elumalai

Abstract: There is an indispensable demand for development of alternative energy sources which would partially or completely replace the utilization of conventional fossil fuels as the combustion of fossil fuels leads to adverse effects on the environmental eco-system. Among electrochemical energy systems, supercapacitors have huge potentials for meeting the power requirements of consumer electronics which require high power. In particular, power density of the conventional lithium-ion battery (LIB) is not suitable, hence, high power device is demanded for hybrid electric vehicles (HEVs) and electric vehicles (EVs). However, low voltage and poor energy density of the supercapacitors are to be upgraded. In this talk, recent progress made on the electrode materials, in particular, oxide-based nanocomposites for high energy and high power supercapacitors/supercapattery would be presented.

Session No: 18 | Session Title: ESD & SoC Design and Verification

Audi: 7 | 04:30 PM-06:00 PM | **Session Chair:** Dr. Rajat Sinha (Micron)
Track: Electrostatic Discharge Reliability (ESD) & ULSI Circuits/System-on-Chip/Power SoC (SoC)
Date: 12-Dec-22

18-1: Practical Strategies for Full Chip ESD checking (Invited Talk)
Start Time: 04:30 PM (30 Mins)
Speaker/Author: Mr. Jonathan White, Synopsys Corp, USA
Presenter: Mr. Jonathan White

Abstract: ESD checking is critical for modern SoC designs. High speed applications, multiple power domains, and shrinking geometries all cause full chip ESD protection schemes to become very complex. It is vital to have a practical and reliable ESD checking methodology for a production design flow. However, design size makes simulation and other traditional ESD checking methods simply impractical or even impossible. This talk presents some strategies used by foundries and EDA vendors to enable realistic full-chip analysis of ESD. The strategies presented will include Rcommon removal (branch point detection), distributed power clamp handling, PG network pruning and others.

18-2: Considerations For ESD Robust Output Driver Design (Invited Talk)
Start Time: 05:00 PM (30 Mins)
Speaker/Author: Mr. Anurag Mittal, Synopsys, India
Presenter: Mr. Anurag Mittal

Abstract: A robust driver structure in an I/O plays a vital role in protection against the ESD events. This study explores various Driver topologies - single MOS structure driver and Multiple MOS stack structures possible for any interface design. The role of breakdown parameters (It2, Vt2) of the driver MOS, Gate conditions, parasitic diodes, common active vs separate active on driver breakdown. We have also explored the use of series resistance along with the driver structure and derived an effective R*W for any driver design. In the end we have summarized the best approach of ESD robustness without compromising I/O functionality based on our I/O design silicon experience.

18-3: Formal Verification: Ready for Rapid Growth (Invited Talk)
Start Time: 05:30 PM (30 Mins)
Speaker/Author: Mr. M V A Kiran Kumar, Intel Fellow, Intel, India
Presenter: Mr. M V A Kiran Kumar

Abstract: The increasing ubiquity and complexity of electronics in the semiconductor industry demands the accurate and accelerated verification of designs. Formal verification has emerged as a promising technique to surpass the shortcomings of the dynamic verification method and ensures complete coverage. Formal methods are applied at different stages of the IP cycle. We present a concise yet informative “Formal Verification Roadmap” which would be of interest to executives and management who are at different levels of embracing formal methods: right from a nascent stage of building a formal centric team all the way until harnessing the power of formal as a mainstream verification methodology.

Session No: 19 | Session Title: Photodetectors
Audi: 8 | 04:15 PM-06:00 PM | **Session Chair:** Dr. Gauri Karwe
Track: Solar Cells & Photodetectors: Physics, Device, & Modules (SP)
Date: 12-Dec-22

19-1: Antimonide based Short Wave Infrared Avalanche Photodiodes for LiDAR applications (Invited Talk)
Start Time: 04:15 PM (30 Mins)
Speaker/Author: Prof. Sanjay Krishna, Ohio State University
Presenter: Prof. Sanjay Krishna

Abstract: A low noise linear mode avalanche photodiodes (LmAPDs) is a critically enabling component for eye-safe long range LiDAR and remote sensing applications. Unlike PIN diodes, APDs provide internal gain that can lead to increased signal to noise ratio and suppress downstream circuit noise. We are investigating two antimonide based multipliers, AlGaAsSb and AlInAsSb, on InP substrates. We have recently demonstrate GaAsSb/AlGaAsSb separate absorber charge and multiplier (SACM) heterostructures . We will discuss the technical challenges associated with the design, growth, fabrication and test of these LmAPDs and the potential for the development of these critical APD arrays for active 3D sensing and imaging systems.

19-2: Design of Electron and Hole Barriers for Type-II Superlattice Absorber for Infrared Photodetection (Oral)
Start Time: 04:45 PM (15 Mins)
Speaker/Author: Anuja Singh (IIT Bombay, India); Bhaskaran Muralidharan (Indian Institute of Technology Bombay, India)
Presenter: Anuja Singh

Abstract: For the construction of the absorber region in infrared photodetectors, type-II Superlattice is favored over traditional HgCdTe due to its band-tunability. The generation-recombination processes that result in noise-inducing currents in these infrared detectors are a significant performance bottleneck, so over the past few years, there have been a lot of research efforts aimed at mitigating these processes to ensure high-temperature operation with improved figure-of-merits. In this work, we showcase the electron and hole barriers for type-II superlattice absorbers to reduce these prime dark current components in infrared photodetectors. Here, we investigate the electronic band properties of InAs/AlSb, GaSb/AlSb, and M-superlattice (InAS/GaSb/AlSb/GaSb) materials as carrier-impending barriers by employing the 8 band k.p method and the non-equilibrium green's function approach. In this article, we demonstrate that InAs/AlSb (GaSb/AlSb) only ever function as a hole (electron)

barrier and never as an electron (hole) barrier. Additionally, we show that we can achieve both the electron and hole barriers by modifying the material widths in the M-superlattice.
19-3: Organic Dye Based Longer Wavelength Photodetector for Narrowband Application (Oral)
Start Time: 05:00 PM (15 Mins)
Speaker/Author: Swati Suman (Indian Institute of Technology, Madras, India); Parasuraman Swaminathan (Indian Institute of Technology Madras, India); Bhola Pal (IIT (BHU), Varanasi, India)
Presenter: Swati Suman

Abstract: The narrowband red-light photodetectors are highly needed selective-color imaging and multi-output visible light communication (VLC). Several organic dyes are being explored for selective narrowband applications in the visible region; its application has yet to be explored in different areas. We have reported a low-cost solution-processed metal oxide (ZnO)-based photodetector. The study is being carried out under white and red lights. When organic dye material is being used on the top of the device and it shows a positive effect under red illumination. This device structure gives the 11.7nA photo-current under red light, while bare ZnO is highly insensitive toward the red spectrum. The functionality of the device structure is checked under white light (one sun) and found an enhancement of 1.8μA. This work demonstrates narrow band optoelectronic application using organic dye with a low-cost solution-processed metal oxide.

19-4: High-Detectivity Ultraviolet Photodetectors With Epitaxial GaN on Si(111) (Oral)
Start Time: 05:15 PM (15 Mins)
Speaker/Author: Pinki Pal, Bhupesh Bhardwaj and Robin Dahiya (IIT Bombay, India); Sami Suihkonen (Aalto University, Finland); Jori Lemettinen (Infinion, Austria); Apurba Laha (Indian Institute of Technology Bombay, India); Dinesh Kabra and Suddhasatta Mahapatra (IIT Bombay, India)
Presenter: Pinki Pal, Bhupesh Bhardwaj

Abstract: Fabrication and systematic characterization of GaN/Si(111)-based visible-blind ultraviolet photodetectors, with Pt/Au contacts, is reported. We demonstrate a record-high detectivity of 4.93x10 14 Jones, for bias voltages exceeding VB = 14 V. The high detectivity is obtained due to extremely low dark current (~ pA, even for VB = 40 V), and high responsivity, in the wavelength range of 320 nm - 380 nm. The highest responsivity obtained for the measured devices is 255 A/W, at VB = 50 V and excitation wavelength of 353 nm.

19-5: Device Engineering for Ga2O3 based High Performance Deep UV Detectors (Invited Talk)
Start Time: 05:30 PM (30 Mins)
Speaker/Author: Dr. Ankush Bag, Indian Institute of Technology Guwahati, India
Presenter: Dr. Ankush Bag, Indian Institute of Technology Guwahati, India

Abstract: Gallium Oxide is an emerging ultra-wide bandgap semiconductor for the detection of deep UV rays around 254 nm. Apart from the direct band gap of ~4.9 eV, there are a few more material advantages of Ga2O3 such as good stability, high absorption coefficient, easier synthesis, etc. Although there have been remarkable developments in this domain across the globe during the last few years, still there are ample scopes for further improvement of these detector performances considering responsivity, the tradeoff between responsivity and dark current, and speed. In this regard, we attempted to improve the performance of these detectors by engineering heterojunction, PN junction, plasmon, etc.

Session No: 20 | Session Title: Advanced photonic integrated circuits
Audi: 9 | 04:30 PM-06:00 PM | **Session Chair:** Prof. Yating Wan
Track: LED & Semiconductor Lasers: Device, Physics & Modules (LL)
Date: 12-Dec-22

20-1: Laser integrated nanophotonics on an InP membrane (Invited Talk)
Start Time: 04:30 PM (30 Mins)
Speaker/Author: Dr. Yuqing Jiao, Eindhoven University of Technology, The Netherlands
Presenter: Dr. Yuqing Jiao

Abstract: Recent progress in the InP membrane on Si (IMOS) platform will be reviewed. This platform features native laser integration with nanophotonic components on a 300nm thick photonic membrane based on InP material system. The twin-guide active-passive integration strategy enables wafer scale high-density integration of amplifiers and lasers. Large scale nanostructures such as metalens can be realized in the same process flow. Thanks to its high optical confinement, novel materials such as phase change materials can be integrated onto the

platform and enable new functions. This technology has high potential for a range of emerging applications including optical wireless communications, non-contact sensing and metrology.

20-2: Silicon nitride photonic platform with integrated source and detectors (Invited Talk)
Start Time: 05:00 PM (30 Mins)
Speaker/Author: Prof. Shankar kumar Selvaraja, Indian Institute of Science
Presenter: Prof. Shankar kumar Selvaraja

Abstract: In this talk, we shall discuss the strategies to integrate silicon and silicon nitride to create a broadband photonics platform. We shall discuss material requirement, device design, fabrication challenges and measurement results of detectors for potential sensor and high-speed communication applications.

20-3: Challenges in Compact Modeling for Integrated Optical Solutions (Invited Talk)
Start Time: 05:30 PM (30 Mins)
Speaker/Author: Dr. Usha Gogineni, ams OSRAM, India
Presenter: Dr. Usha Gogineni

Abstract: Optical sensors are omnipresent in electronic devices and equipment used in the consumer, automotive, industrial and medical fields. Integrating these sensors into CMOS technologies leads to a unique set of challenges to the compact modeling of the sensors, as well as the other semiconductor devices used in the read-out circuitry. This talk will focus on the modeling challenges pertaining to the optical solutions in the consumer space, including proximity sensors, ambient light sensors, time of flight sensors and CMOS image sensors.

Session No: 21 | Session Title: Silicon Stays Strong
Audi: 10 | 04:30 PM-06:00 PM | **Session Chair:** Dr. Madhur Bobde
Track: Advanced Power Device Technology (APDT)
Date: 12-Dec-22

21-1: How Silicon Power Devices are withstanding the onslaught from WBG Devices (Invited Talk)
Start Time: 04:30 PM (30 Mins)
Speaker/Author: Mr. Dhaval Dalal, ACP Technologies
Presenter: Mr. Dhaval Dalal

Abstract: With interesting new technological developments in power semiconductors, a lot of focus has been on the WBG devices and their promised performance enhancements. However, the tried and tested silicon devices are still holding their own and their longevity is attributable to continuing advances in both device technology and packaging technology that make them attractive to the end users in the power electronics community. Some of these recent technology advances will be outlined in this talk, accompanied by examples of how they are enabling more energy efficient, compact and cost-effective power conversion solutions.

21-2: Use Cost per Ampere delivered ($/ARMS) as a Design Decision Metric for Selecting Power Devices (Invited Talk)
Start Time: 05:00 PM (30 Mins)
Speaker/Author: Mr. Vijay Bolloju, India
Presenter: Mr. Vijay Bolloju

Abstract: With many device technologies available today, it is difficult for designers to choose a device using just the data sheet parameters. Different device technologies have different trade-offs between conduction, switching parameter and thermal performance. Using these parameters to select a device gets complex.
RMS current delivered by a device is a result of the losses generated by it and its thermal performance so, using it to select a device will optimize the choice. Further, best cost-performance balance can be optimized by comparing cost per Ampere ($/ARMS) delivered using the cost of the devices. We will present some examples in this paper.

21-3: Advanced Power Devices Packaging (Invited Talk)
Start Time: 05:30 PM (30 Mins)
Speaker/Author: Prof. Soumya Shubhra Nag, Indian Institute of Technology Delhi
Presenter: Prof. Soumya Shubhra Nag

Abstract: Si-MOSFET/IGBT finds wide application in personal computers, servers, micro-inverters, motor-drives, telecom systems, etc. Advent of WBG semiconductor technology has not been able to replace the Si Technology. However, due to the aggressive needs of the power management systems in terms of higher power-density, lower parasitic-inductance, lower thermal-resistance, Si semiconductor industry is still going through innovations to keep the performance of devices at optimum level.
Recent improvements in Si-device packaging technology have significantly optimized device parameters and figure-of-merits (RDS(ON)*Qg, Qrr, Esw). Furthermore, with the increase in system current requirements, optimization of these device parameters become important which resulted in advent of packages like DPAK, D2PAK, SO-8, CopperStrapTM SO-8, PowerPakTM, LFPAKTM, DirectFETTM, TOLL, sTOLL, etc. This talk will elaborate the evolution and trends in packaging technologies for achieving better device characteristics which can enable high performance product designs for automotive, energy, data center applications.

Session No: 22 | Session Title: Design Automation in Advanced Technologies
Audi: 11 | 04:30 PM-06:00 PM | **Session Chair:** Dr. Rahul Rao
Track: Advanced Logic Technologies (ALT)
Date: 12-Dec-22

22-1: Gate-All-Around Nanosheet Device Options for Multi-Node Extendibility (Invited Talk)
Start Time: 04:30 PM (30 Mins)
Speaker/Author: Dr. Krishna K. Bhuwalka, Huawei Technologies R&D, Belgium
Presenter: Dr. Krishna K. Bhuwalka

Abstract: We investigate nanosheet family of devices for logic CMOS scaling at 3nm and beyond using full design-technology co-optimization framework. FinFETs, gate-all-around (GAA) nanosheets (NS)-FETs and fork-sheets (FS)-FETs options are benchmarked. While GAA NS provide better performance and gate-length scaling than FinFETs, additional process optimization by decoupling inner- and outer-gate lengths can result in added gate-length scaling flexibility. Impact of vertical pitch is further investigated, especially considering impact of work-function mismatch between inner- an outer-gates at aggressively scaled vertical pitch. It is observed, that up to 200meV work-function difference between inner-outer gates, devices still perform better at 11nm pitch as compared to 15nm pitch.

22-2: Design Automation for concurrent design in emerging technologies (Invited Talk)
Start Time: 05:00 PM (30 Mins)
Speaker/Author: Mr. Arun Joseph, IBM, India
Presenter: Mr. Arun Joseph

Abstract: With the drive to sustainable reliable IT, the onus for extracting the maximum performance from technology migrations lies in newer design paradigms, and methodologies. In this talk will highlight some emerging technology trends, and illustrate its implications to hardware design, specifically high performance chip design, which in terms necessitates innovation in Electronic Design Automation (EDA). I will delve more into challenges in characterization of timing, power, noise, and reliability. I will also highlight some Cloud & AI/ML techniques leveraged for efficient industry scale designs, before concluding with how these tie into a concurrent design philosophy of hardware design.

22-3: Towards extreme scaling of CMOS technology using Forksheet and CFET (Invited Talk)
Start Time: 05:30 PM (30 Mins)
Speaker/Author: Dr. Pieter Weckx, IMEC Belgium
Presenter: Dr. Pieter Weckx

Abstract: Scaling below 3nm will bring us far into the post FinFET era where extremely scaled logic standard cell heights and SRAM will limit the nanosheet scalability. The novel forksheet device architecture has been proposed as an ultimate scaling device towards 2nm and beyond. Furthermore, complementary FETs (CFETs) offer promise of ultimate scaling beyond the 1nm node and the ability to integrate alternate high mobility channels. Beyond CFETs, 2D materials such as MoS2, WS2 or HfS2 can be used to form atomic channel transistors, offering high mobilities and gate length scaling potential.

Session No: 23 | Session Title: Fundamentals of 2D devices 1
Audi: 1 | 11:15 AM-12:30 PM | **Session Chair:** Prof. Yashowanta N Mohapatra
Track: 2D Material Based Technologies (2DT)
Date: 13-Dec-22

23-1: The requirement for 2D functional materials to solve today's challenging Engineering problems (Invited Talk)
Start Time: 11:15 AM (30 Mins)
Speaker/Author: Mr. Ajay Kumar Vaidhyanathan, Intel, India
Presenter: Mr. Ajay Kumar Vaidhyanathan

Abstract: At present we are facing insurmountable challenges in solving engineering issues in many engineering domains. For example, Thermal, Mechanical, EMI, Power integrity, signal integrity etc. The unique properties of 2D materials have the potential breakthrough solution in these engineering domains. Another advantage of this is we can modify their functional characteristics depending on our needs. One of the major challenges at present we are facing to adapt this technology, is due the challenges we face in High Volume Manufacturing. In this presentation I will be discussing the need, Examples of how we are trying to adapt in engineering design, Critical need for University-Academia coloration etc.

23-2: Key Components of Contact Resistance to Atomically Thin Semiconductors and Requirements for Their Reduction (Invited Talk)
Start Time: 11:45 AM (30 Mins)
Speaker/Author: Prof. Eilam Yalon, Technion - Israel Institute of Technology, Israel
Presenter: Prof. Eilam Yalon

Abstract: Achieving good electrical contacts is one of the major challenges in realizing devices based on atomically thin two-dimensional (2D) semiconductors. Several approaches have been proposed to reduce contact resistance, including clean contacts, doping, phase engineering, edge contacts, 2D contacts, van der Waals (vdW) contacts, and semimetal contacts. Nonetheless, a better understanding of the fundamental mechanisms limiting the electrical contact resistance to atomically thin 2D semiconductors is needed. This talk will revisit the classical transmission line model description of contacts to 2D materials, present experiments and simulations that uncover the key components of contact resistance to 2D semiconductors and provide guidelines for their reduction. The presented findings can explain recently published state-of-the-art results and offer insight for future contact engineering.

23-3: Performance of Two-Dimensional MoS2 Field-Effect Transistor in the Presence of Oxide-Channel Imperfection (Oral)
Start Time: 12:15 PM (15 Mins)
Speaker/Author: Akhilesh Rawat (Indian Institute of Technology Ropar, India); Anjali Goel (Indian Institute of Technology, Ropar, India); Brajesh Rawat (IIT Ropar, India)
Presenter: Akhilesh Rawat (Indian Institute of Technology Ropar, India); Anjali Goel (Indian Institute of Technology, Ropar, India); Brajesh Rawat (IIT Ropar, India)

Abstract: In this work, we propose a more accurate description of the interface trap in the MoS_2 field-effect transistor using a quantum-mechanical modeling framework. Introducing an interface trap based on tight-binding parameter substitution at an atomic site is found to be a more effective way to include its effect on the device electrostatics and the carrier transport. Further, lower energy interface traps from conduction band are found to significantly impact the device performance, with severe degradation in subthreshold slope and ON-current. Our proposed model reveals that charge trapping in the interface trap causes substantial degradation in the drive current for high gate biases, whereas source-to-drain tunneling through trap limits the performance for low gate biases.

Session No: 24 | Session Title: High Frequency Measurements and Modelling
Audi: 2 | 11:15 AM-01:00 PM | **Session Chair:** Prof. Yogesh Chauhan
Track: Modelling and Simulations (MS)
Date: 13-Dec-22

24-1: RF Modeling challenges for emerging technologies (Invited Talk)
Start Time: 11:15 AM (30 Mins)
Speaker/Author: Mr. Ananth Sundaram, Globalfoundries India Pte Ltd
Presenter: Mr. Ananth Sundaram

Abstract: With both evolutionary and disruptive changes in standards for wireless communications, the prediction of device behavior under regular and extreme conditions has become critical for designers to get first time right products. It's no longer enough to be accurate in current, voltage and transconductance predictions but it's a need to predict non-linearities accurately as well. We will talk about some of these challenges in this talk.

24-2: Modeling of N-polar GaN heterostructures and transistors (Invited Talk)
Start Time: 11:45 AM (30 Mins)
Speaker/Author: Dr. Arvind Ajoy, Indian Institute of Technology Palakkad, India
Presenter: Dr. Arvind Ajoy

Abstract: N-polar GaN offers significant advantages over Ga-polar GaN. For example, transistors realized with N-polar GaN have demonstrated record values high of power density, operating frequency and record low values of ON-resistance [1]. Most of the modeling efforts have focused on the Ga-polar orientation. We show that the key approximations involved in the modeling of Ga-polar devices need to be revisited while modeling N-polar devices. Based on these observations, we present analytical [2] and closed form models to describe the wavefunctions, surface potential and charge in N-polar heterostructures. We also present an extension of this modeling approach to describe the current-voltage characteristics of N-polar GaN transistors.

[1] M. H. Wong and U. K. Mishra, "N-polar III-nitride transistors," in Semiconductors and Semimetals, vol. 102. Amsterdam, The Netherlands: Elsevier, 2019, pp. 329–395
[2] Anuja Menokey and Arvind Ajoy, "Air Function Based Model for 2-DEG Charge and Surface Potential in N-Polar Gallium Nitride Heterostructures," vol 59, IEEE Trans. Electron Devices, 2022, pp. 3861 – 3868.

24-3: Compact 2-RC Model for Lateral NQS Effects in SiGe HBTs (Oral)
Start Time: 12:15 PM (15 Mins)
Speaker/Author: Sandip Ghosh (Indian Institute of Technology Madars, India); Shon Yadav (Global Foundries, India); Anjan Chakravorty (IIT Madras, India)
Presenter: Sandip Ghosh

Abstract: A physics-based model is proposed to accurately capture the lateral non-quasi-static (LNQS) effects in SiGe HBTs. The model uses new methodology to implement the internal base impedance of the device using two-RC circuits. Equations of all base impedance-related components associated with the two-RC network are derived. The proposed model is implemented in Verilog-A. The small-signal AC and the large-signal transient simulations show that the two-RC model yields significantly more accurate results when compared with those of the state-of-the-art model and the π-model.

24-4: Calibration kit design for high Frequency measurement (Invited Talk)
Start Time: 12:30 PM (30 Mins)
Speaker/Author: Dr. Chandan YADAV, National Institute of Technology Calicut, Kerala, India
Presenter: Dr. Chandan YADAV

Abstract: Accurate, reliable and repeatable measurement of semiconductor devices is essential for high frequency device modeling to circuit and system design. The talk will be focused on role of EM simulation in calibration kit design for measurement of semiconductor devices for high frequency measurement.

Session No: 25 | Session Title: WBG device based Power Electronics Applications

Audi: 3 | 11:15 AM-01:15 PM | **Session Chair:** Dr. Kamal Varadarajan
Track: Wide Bandgap Device Based Circuits and Systems (WDCS)
Date: 13-Dec-22

25-1: WBG vs Silicon Transistors in AC/DC Converters (Invited Talk)
Start Time: 11:15 AM (30 Mins)
Speaker/Author: Mr. Roland Saint-Pierre, Power Integrations
Presenter: Mr. Roland Saint-Pierre

Abstract: Silicon has been the workhorse of the industry for power conversion for many decades and will continue to be employed for many years to come. Wide bandgap transistors offer huge advantages in pushing the power density and efficiency to new heights. The improved performance of WBG transistors enables smaller and lighter power adapters and embedded conversion stages. These performance improvements are required to meet ever demanding regulatory mandates for higher efficiency. It is important that manufacturers ensure a seamless user

experience to promote widespread adoption. This requires system optimization with advanced control features to maximize system benefits. The presentation compares silicon, GaN and silicon-carbide (SiC) device application in a variety of AC/DC power converters.

25-2: Reinventing Power Electronics: NexGen Power Systems with NexGen Vertical GaN™ (Invited Talk)
Start Time: 11:45 AM (30 Mins)
Speaker/Author: Dr. Dinesh Ramanathan, NexGen Power Systems, US
Presenter: Dr. Dinesh Ramanathan

Abstract: NexGen Power Systems brings to the market the world's smallest, lightest, and most efficient power systems that are based on its unique and proprietary GaN-on-Gan power semiconductor technology, NexGen Vertical GaN™. Not only does NexGen Vertical GaN™ provide all the benefits of what a perfect power semiconductor should have: High Switching Frequency, High Voltage, stable on-resistance, low-temperature coefficient, single and repetitive avalanche capability, and >10µs short-circuit protection. Furthermore, these power systems are based on NexGen's scalable, software-configurable power platform that unlocks the true potential of the semiconductor technology and re-invents power electronics.

25-3: Integration Choices in Power GaN HEMT (Invited Talk)
Start Time: 12:15 PM (30 Mins)
Speaker/Author: Dr. Amitava Das, Tagore Technology Inc
Presenter: Dr. Amitava Das

Abstract: Wide bandgap semiconductors, such as GaN, are winning designs in the power supply market. Power supply designers have multiple options, such as using standalone GaN FET, GaN FET with integrated driver or GaN FET power module. GaN FET with integrated driver can be monolithic or heterogenous integration of two die – a GaN die and a CMOS driver die. This talk will review various integration options and highlight tradeoffs between them.

25-4: Integrating Silicon Driver with GaN Transistor Simplifies Power System Design and Enhances Performance (Invited Talk)
Start Time: 12:45 PM (30 Mins)
Speaker/Author: Dr. Prasanna Udupi Rajagopal, Texas Instruments, Bangalore
Presenter: Dr. Prasanna Udupi Rajagopal

Abstract: GaN (Gallium Nitride) transistors can switch at much higher rate as compared to Silicon MOSFETs while bringing in advantages of lower switching losses and reduce system size. However, switching at higher slew rate poses challenges in terms of switching performance due to parasitic common-source inductances. This presentation talks about advantages of integrating silicon driver with the GaN FET in an integrated package to optimize the gate loop to enable excellent switching performance at slew rates above 100V/ns. In addition, the package integrates protection features like over current/short circuit protection and monitoring junction temperature to simplify power converter designs.

Session No: 26 | Session Title: Biosensors 2

Audi: 4 | 11:15 AM-01:00 PM | **Session Chair:** Prof. Ambarish Ghosh
Track: Sensors and Bio-Electronics (SBE)
Date: 13-Dec-22

26-1: Electronic skin - sensing the world around us and within us (Invited Talk)
Start Time: 11:15 AM (30 Mins)
Speaker/Author: Prof. Madhu Bhaskaran, RMIT University, Melbourne, Australia
Presenter: Prof. Madhu Bhaskaran

Abstract: The presentation will focus on stretchable and wearable electronics which represents a new wave in devices which can bend, flex, and stretch. My work seeks to transform conventional hard electronics into soft and unbreakable products, thin enough to create electronic skin. We realise thin electronic patches that adhere to the skin that can mimic body functionality, measure and diagnose, monitoring environment around, on, and within us. These next-gen stretchable electronics for a diverse range of current and visionary applications are being commercialised with Australian industry. Examples include skin-worn sensors to warn people about harmful UV and nicotine levels, wearables for health monitoring, and nearables in bedding.

The presentation will cover the decade long journey to realise conformal electronics - these include the fundamental research to solve technical challenges to integrate high performing rigid oxide materials with soft polymeric rubber platforms. Besides the applied outcomes, the fundamental research has also helped push the boundary on creating artificial somatosensors - electronic skin which mimics the properties of real skin.

26-2: Electrolyte-Gated WSe2 Field Effect Transistor for Dissolved Ammonia Sensing in Human Plasma (Oral)
Start Time: 11:45 AM (15 Mins)
Speaker/Author: Sumit Sharma (Indian Institute of Technology Delhi & Center for Applied Research inn Electronics, India); Akshay Moudgil, Sanjay Singh and Prashant Mishra (Indian Institute of Technology Delhi, India); Samaresh Das (IIT Delhi, India)
Presenter: Sumit Sharma

Abstract: The development of a highly sensitive electrolyte gated field-effect transistor (EGFET) is based on layered transition metal dichalcogenides (TMDs). The FETs based on layered TMDs are considered as a possible alternative for biosensing applications because of their superior electrical and physical characteristics. In this work, a highly efficient few-layer WSe2 EGFET is fabricated for dissolved ammonia detection in plasma. The sensors respond extremely well to ammonia in plasma at concentrations of 80 μM and 5 μM, respectively, with responses of 157% and 98%. These findings demonstrate the possibility of ammonia detection in human blood plasma obtained from commercial sources.

26-3: Electrochemical Detection of Catechol Using Biochar/Copper Oxide Nanoparticles Layered at Carbon Paste Electrode (Oral)
Start Time: 12:00 PM (15 Mins)
Speaker/Author: Pavithra N (INDIAN INSTITUTE OF SCIENCE, India); Radhika Varshney (Indian Institute of Science, Bangalore, India); T S Sunil Kumar Naik, Simranjeet Singh and Praveen C Ramamurthy (Indian Institute of Science, India)
Presenter: Pavithra N

Abstract: Catechol (CA) is dihydroxy benzene isomer that reacts with biomolecules and causes damage to human health. Therefore, an electrochemical sensor for catechol is developed based on novel biochar/copper oxide nanoparticles (BC/Cu) modified carbon paste electrode. The characterization of BC/Cu is performed by UV spectroscopy, FTIR, and SEM-EDS. The modified electrode can detect CA in a wide range from 10-100 μM in PBS buffer with a limit of detection of 1.03 μM. The selectivity of the electrode was tested with common interfering molecules, and stability was estimated in terms of days which showed excellent selectivity and long-term stability. Therefore, this sensing material can be effectively used to detect CA by electrochemical technique.

26-4: Design and Fabrication of Droplet Based Microfluidic Device for Wearable Sensing (Oral)
Start Time: 12:15 PM (15 Mins)
Speaker/Author: Surya Manisha Inukonda (Indian Institute of Technology Kanpur, India)
Presenter: Surya Manisha Inukonda

Abstract: The advent of wearable devices has recently received a lot of attention since it allows for non-invasive monitoring of a range of biomarkers present in biofluids. These devices still have a lot of obstacles to overcome, such as those related to continuous analyte collection. Here, we present a wearable device that combines a flexible substrate with open microfluidic framework for effective analyte collection. The design of the microfluidic system is based on a simple wettability patterning technique, which combines channel design with super-hydrophilic and super-hydrophobic zones to generate unidirectional droplet transport to fill the collection reservoir. This concept was developed using a mixture of hydrophobic polymer and photocatalytic TiO2 nanoparticles as a coating surface. These nanoparticles not only assist in making the surface super-hydrophobic by adding roughness features but also aid in converting the surface from super-hydrophobic to super-hydrophilic state when exposed to UV light. The selective wettability conversion on the surface was accomplished using a photomask with a desired geometric pattern. The characteristics of the manufactured device were investigated using a variety of characterization techniques. A high-speed camera operating at a frame rate of 2000 (fps) was used to record the droplet transportation along the channel's length for optimization of the device parameters. A collection pattern with optimized dimensions was created, and the fabricated device was found to collect approximately 100 (μL) of analyte sample in 5-10 (min).

26-5: Miniaturised electrochemical sensors for in vivo biochemical monitoring (Invited Talk)
Start Time: 12:30 PM (30 Mins)
Speaker/Author: Prof. Pankaj Vadgama, Queen Mary University of London, UK
Presenter: Prof. Pankaj Vadgama

Abstract: Selected biochemical variables are subject to rapid change in the body and justify continuous monitoring. We developed sterilized tissue implantable O, glucose and lactate needle electrodes for short term use. Membrane capping and enzyme (glucose/lactate oxidase) functionalization allowed reliable monitoring with presented a quite distinct physiological compartment with local blood flow overriding circulatory changes in pO2 during exercise, glucose demonstrating a dynamic lag and recovery and lactate subject to a tissue-blood barrier. Additional monitoring of sweat lactate showed only a qualitative ling with exercise whilst salivary lactate tracked blood lactate. Such devices offer a route to better understanding blood-tissue interrelationships.

Session No: 27 | Session Title: OLEDs and Display Technology
Audi: 5 | 11:15 AM-01:00 PM | **Session Chair:** Prof. Dinesh Kabra
Track: Macroelectronics & Displays: Devices, Circuits & Systems (DIS)
Date: 13-Dec-22

27-1: Breaking the Light Outcoupling Efficiency Limit in Perovskite Quantum Dots LEDs Featuring Anisotropic Nanocrystals Superlattices (Invited Talk)
Start Time: 11:15 AM (30 Mins)
Speaker/Author: Dr. Sudhir Kumar, ETH Zurich, Switzerland
Presenter: Dr. Sudhir Kumar

Abstract: Colloidal lead halide perovskites (LHPs) are emerging as one of the most promising classes of light-emitting semiconductors for next-generation displays. However, their intrinsic light outcoupling efficiency remains considerably lower than the organic counterpart, because it is not yet possible to control the transition-dipole-moment (TDM) orientation in QD solids at the device level. Here, we obtain horizontal TDM orientation in the individual anisotropic nanocrystal (ANC) that remains intact in the ANC superlattice (ANSL) without influencing the photoluminescence quantum yield (PLQY) by controlling the aspect ratio of ANCs. Our optimized perovskite light emitting diodes (LEDs), comprising ANSLs thin films with near-unity PLQY, showed record high external quantum efficiency of ~25% and a current efficiency of 103 cd/A.

27-2: Inkjet Printed OLED Displays :Progress and Challenges (Invited Talk)
Start Time: 11:45 AM (30 Mins)
Speaker/Author: Prof. Monica Katiyar, IIT Kanpur, India
Presenter: Prof. Monica Katiyar

Abstract: Inkjet printing (IJP) is a promising emerging technology, but it has many challenges, inherent limitations, and advantages. This presentation aims to understand the challenges and exploit the advantages to develop low-cost displays using IJP. Three case studies are presented for light-emissive layers: small molecules, a thermally activated delayed fluorescent (TADF) materials, and light-emitting polymers. The inkjet printing technique is used to deposit the SU-8 in the desired pattern, eliminating the photolithography step for pixelization. An inkjet-printed silver electrode on flexible substrates is also developed as a replacement for indium tin oxide (ITO). In summary, our results show the potential for fabricating large-area OLEDs using inkjet printing technology, potentially paving the way for a new generation of flexible, low cost, and low power displays.

27-3: Challenges and Approaches Towards Defect Free Large Area Organic Light Emitting Diode Fabrication (Oral)
Start Time: 12:15 PM (15 Mins)
Speaker/Author: Madhu Seetharaman (Indian Institute of Technology- Kanpur, India); Gopika Pillai, Rita Rana and Asha Awasthi (Indian Institute of Technology Kanpur, India); Krishna Manohara (Indian Institute of Technology- Kanpur, India); Muralidharan Balakrishnan (Indian Institute of Technology Kanpur, India); Monica Katiyar (IIT Kanpur, India)
Presenter: Madhu Seetharaman

Abstract: Large area Organic Light Emitting Diodes (OLEDs) are promising candidates for next generation solid state lighting application, with very good efficiencies and performances. OLED unit consists of very thin layers of organic materials over a large area and the major challenge remains in the fabrication of large area devices without defects, which cause sudden failure. Phosphorescent OLED devices were fabricated with an emissive area

of 8 cm2 x 8 cm2 and various factors contributing to the formation of defects and non-uniformity were identified and mechanism of short formation was studied. Further improvements were incorporated in the device fabrication to achieve defect free OLED panels.

27-4: Next-Generation Technologies for AMOLED Display Manufacturing (Invited Talk)
Start Time: 12:30 PM (30 Mins)
Speaker/Author: Dr. RAJESWARAN, Gopalan, Indian Institute of Technology Madras
Presenter: Dr. RAJESWARAN, Gopalan

Abstract: The Organic Light Emitting Diode (OLED) device was invented by Ching Tang and Steve VanSlyke at Kodak Research Laboratories in 1987 and the first full color AMOLED display was developed and demonstrated by Rajeswaran et al in 1999. The first commercial AMOLED displays were delivered in 2002 by SK Display, a Kodak-Sanyo joint venture. By 2020, the AMOLED industry had grown to $30 billion in market size. The recent commercial success of flexible AMOLED displays signals the promise of further growth in the AMOLED display industry. The current generation of vacuum-deposited, small-molecule AMOLED displays utilizes either the Fine Metal Mask (FMM) method or the White OLED plus integrated RGB color filters (WRGB) method for creating the primary color sub-pixels. The FMM method is now widely used in the production of AMOLED displays for smartphone applications while the WRGB method is used for the manufacture of OLED TVs. This talk will review the several drawbacks in the current OLED production technologies, namely, substrate size limitation in OLED patterning, poor materials utilization and low productivity. The prospects of overcoming these limitations with a new method of organic materials delivery called close space sublimation will be explored and early results will be reviewed. A state-of-the-art AMOLED display development facility has been set up at the Indian Institute of Technology Madras to explore next-generation manufacturing technologies based on the close space sublimation of organic materials. India has now emerged as the 2nd largest global market for mobile phones and the prospects look attractive for the emergence of an AMOLED display manufacturing industry in India.

Session No: 28 | Session Title: Electrochemical Mechanism and Interfaces
Audi: 6 | 11:15 AM-01:00 PM | **Session Chair:** Dr. Aiswarya Bhaskar
Track: Energy Storage and Batteries (ESB)
Date: 13-Dec-22

28-1: Bipolar lithium-metal battery employing a quasi-solid composite electrolyte (Invited Talk)
Start Time: 11:15 AM (30 Mins)
Speaker/Author: Dr. Dominic Bresser, Karlsruhe Institute of Technology (KIT)
Presenter: Dr. Dominic Bresser

Abstract: Lithium metal is considered as one of the most promising anode candidates for high-energy batteries. However, safety concerns induced by the formation of Li dendrites hinder the practical application. Herein, we report on a thin and flexible hybrid electrolyte composed of Li1.3Al0.3Ti1.7(PO4)3 (LATP), a polymer binder, and a small amount of an ionic liquid-based electrolyte. To reinforce the interfacial stability between LATP and Li, we coat an ultrathin polysiloxane-based single-ion conducting polymer on the lithium surface. This enables a substantial performance improvement of Li‖LiNi0.88Co0.09Mn0.03O2 cells, eventually enabling the successful realization of lab-scale bipolar stacked battery cells.

28-2: High-Capacity Organic Redox Flow Battery (Invited Talk)
Start Time: 11:45 AM (30 Mins)
Speaker/Author: Prof. Kothandaraman Ramanujam, Professor
Presenter: Prof. Kothandaraman Ramanujam

Abstract: To combat global warming, redesigning of the world energy-consuming structure is imminent. India's solar power tariff has fallen below 3.2¢/kWh, and the international tariff of solar thermal storage power is US$0.063/kWh, which are cheaper than that of fossil fuel plants. Therefore, in the future, solar power cost will become the benchmark for deciding the other fuel prices. Renewables sources are seasonal, therefore there is a requirement for low cost energy storage option to store the excess energy for prolonged time period. Considering the longevity, capacity, availability of raw materials and safety, non-flammable aqueous electrolyte-based redox flow batteries are the choice.

28-3: Room Temperature Fabrication of MnO2-Based Printable and Flexible Microsupercapacitors (Oral)
Start Time: 12:15 PM (15 Mins)
Speaker/Author: Sushree Sangita Priyadarsini (Indian Institute of Science, Bangalore, India); Subho Dasgupta (Indian Institute of Science (IISc), Bangalore, India)
Presenter: Sushree Sangita Priyadarsini

Abstract: Wearable electronics require reliable, light weight, efficient, easy-to-integrate and mechanically compliant power sources. The increasing energy demand in emerging wearable and portable electronic devices has resulted in emergence of a new research area, namely, microsupercapacitors (MSCs), which are compact, high energy density, miniaturized supercapacitor units. In this study, ε-MnO2 nanoflowers (NFs) have been synthesized by chemical reduction of KMnO4. A printable ink formulated with these nanoflowers and deposited onto Sn-doped indium oxide (ITO) coated PET (polyethylene terephthalate) exhibits a specific capacitance of 384 F/g under the 3-electrode measurement setup. Next, the ultrathin, flexible, lightweight symmetric MSCs fabricated with ε-MnO2 nanoflowers has demonstrated specific gravimetric capacitance of 111.5 F/g at a voltage scan rate of 2 mV/s with a potential window of 2 V. The gravimetric energy density and power density of these MSCs have been estimated as 38.4 W.h/kg and 10 kW/kg at specific current of 0.5 A/g and 10 A/g, respectively. In addition, the areal capacitance value has been estimated as 3.9 mF/cm 2 .

28-4: Endeavoring to make a solar battery (Invited Talk)
Start Time: 12:30 PM (30 Mins)
Speaker/Author: Prof. Deepa Khushalani, Tata Institute of Fundamental Research
Presenter: Prof. Deepa Khushalani

Abstract: Devising energy schemes that merge energy capture with energy storage have gained momentum over the last few years. The impetus stems from utilizing solar radiation efficiently in terms of not only capturing it but also viably storing it in the form of either solar fuels or as electrical storage. The latter technology is still emerging especially in terms of evolving the conceptual idea of directly storing solar radiation as opposed to forming devices that consist of independent batteries/supercapacitors that are separately coupled with solar cells. Hence it can be considered that the integrated system is composed of two kinds of materials: light harvesting and a storage component. Light harvesting component consists of materials that are capable of absorbing light and generating extractable charge carriers, while, energy storage component consists of materials that can trap the charges and store them during periods of illumination, and subsequently release them under discharge conditions.
The talk will present some concepts that are currently available in literature as to how to form such integrated systems and I will also discuss our work where we have used an alternate strategy for coupling energy capture and storage in that the aim has been to create a strategy that minimizes interfaces and so in principle can lead to better performance and charge transport efficiency.

Session No: 29 | Session Title: THz spectroscopy for Materials

Audi: 7 | 11:15 AM-12:45 PM | **Session Chair:** Dr. Dibakar Roy Chowdhury
Track: RF, Millimeter and THz Technologies, Circuits and Systems (RF-THz)
Date: 13-Dec-22

29-1: Terahertz quasiparticle excitations in complex oxides (Invited Talk)
Start Time: 11:15 AM (30 Mins)
Speaker/Author: Prof. Dhanvir Singh Rana, Indian Institute of Science Education and Research Bhopal, India
Presenter: Prof. Dhanvir Singh Rana

Abstract: The implementation of terahertz (THz) spectroscopy to unravel the complexity of correlated materials has delivered unprecedented success. In this talk, I'll present some of the achievements including demonstration of novel quasiparticles such as magnons, eletromagnons, charge-density waves (CDW), Dirac and Weyl fermions, trimerons, Higgs mode, magnetic monopole, etc, primarily in transition metal oxides. This diversity of examples underpin THz spectroscopy as indispensable tool for probing a variety of emergent quasiparticles emerging from electrodynamics of collective, bound and free charge carriers, topological phase, complex spin orders, etc, and their applications in electronic and magnonic photonics in the new era of quantum matter.
29-2: Design and Analysis of Programmable Cross-Polarization Converter in Terahertz Band Using Photo-Excited Split-Ring Resonator Based Metasurface (Oral)
Start Time: 11:45 AM (15 Mins)
Speaker/Author: Anirban Chaudhuri (Tata Consultancy Services Limited, India); Parama Pal (TCS Research and Innovation, India)
Presenter: Anirban Chaudhuri

Abstract: Metamaterials and metasurfaces are key components in a wide range of terahertz systems due to their ability to control electromagnetic waves in unprecedented ways and very small size. Metasurface based polarization converters are envisioned to be an integral part of 6G and beyond wireless communication systems. In this work, we have designed a novel programmable metasurface cross-polarization converter based on photo-excited split-ring resonator operating around 1 THz. By varying the conductivity of photoconductive silicon, we achieved a tunability of 20 GHz, while maintaining a PCR greater than 0.9. We have also analyzed how the photoconductive elements change the current flowing through the structure and affect the resonances. The proposed structure is simulated in frequency domain, via finite element method.

29-3: Breast Cancer Detection With Metamerial Enabled Monopole Antennas Using Microwave Imaging (Oral)
Start Time: 12:00 PM (15 Mins)
Speaker/Author: Athul O Asok, Mohammad Abdul Shukoor and Sukomal Dey (Indian Institute of Technology Palakkad, India)
Presenter: Athul O Asok

Abstract: This work introduces a miniaturized monopole antenna based on metamaterials for breast cancer detection. The proposed antenna is designed on a low-cost FR4 substrate with a dielectric constant of 4.4, loss tangent 0.025 and thickness of 1.6 mm. For gain enhancement, the designed antenna is equipped with a frequency selective surface (FSS) on its back side. The suggested antenna obtains a broad bandwidth (S11 > 10 dB) between 3.4 and 9 GHz, with a peak gain of 6.2 dBi at 5 GHz. The proposed work also achieves a maximum gain enhancement of 4.7 dBi with the addition of FSS at the back side of the antenna. The Specific absorption Rate (SAR) study of the antenna with a realistic hemispherical breast phantom modelled in the simulator is performed to assess the impact of radiation on the human breast. It is observed that the proposed antenna complies with the International limits when averaged over 10g of tissue.

29-4: Up-conversion of terahertz phonons via nonlinear coupling (Invited Talk)
Start Time: 12:15 PM (30 Mins)
Speaker/Author: Dr. Rajeev N Kini, IISER Thiruvananthapuram, India
Presenter: Dr. Rajeev N Kini

Abstract: In this work, we demonstrate dynamic control of the lattice by using THz radiation. We use THz pulses with intense electric fields (~ kV/cm) to induce lattice non-linearities, which allow us to couple the low energy phonon modes to higher energy, silent optical phonon modes at ≈ 1.17 THz in the spin-ladder system, Sr14Cu24O41. Due to the coupling, we observe an enhancement in the transmission spectrum, i.e., transmittance > 1, near 1.17 THz. Hence, we demonstrate that it is possible to control inaccessible phonon modes with THz radiation indirectly. This provides opportunities to alter such material systems' electronic and magnetic properties dynamically using THz radiation.

Session No: 30 | Session Title: Quantum Device Technologies

Audi: 8 | 11:15 AM-01:00 PM | **Session Chair:** Prof. Neeraj Khare (IITD)
Track: Quantum Device Technologies (QDT)
Date: 13-Dec-22

30-1: Error mitigation for noisy quantum processors: a path to quantum advantage (Invited Talk)
Start Time: 11:15 AM (30 Mins)
Speaker/Author: Dr. Abhinav Kandala, IBM, USA
Presenter: Dr. Abhinav Kandala

Abstract: Quantum processors based on superconducting circuits have now reached a scale that is well beyond direct diagonalization. However, in the absence of fault tolerance, the central question is whether such noisy processors can provide useful computations. In this context, error mitigation techniques can provide access to noise-free observables even from today's noisy processors. I will introduce these techniques, discuss the current state of quantum hardware and recent experimental results, and chart out an immediately accessible path to quantum computational advantage.

30-2: Fluorescent Nanodiamonds as Quantum Sensors: Effects of Infrared Illumination (Oral)
Start Time: 11:45 AM (15 Mins)
Speaker/Author: Souravi Mukherjee and Eklavy Vashist (INDIAN INSTITUTE OF SCIENCE, India); Ambarish Ghosh (Indian Institute of Science, India)
Presenter: Souravi Mukherjee

Abstract: Nitrogen-vacancy (NV) centers in nanodiamonds (NDs) have emerged as powerful quantum sensors, with diverse capabilities in nano-scale sensing of physical quantities (like temperature, magnetic or electric fields), even in the fluidic medium. We, in this work, study the effects of continuous infrared (IR) illumination on ND photoluminescence (Pl) and the simultaneous effects on the contrast in optically detected magnetic resonance (ODMR) signal. Our study suggests a similar decreasing trend in both the Pl and the ODMR contrast with increasing IR powers. The dependence of ODMR contrast on IR power is seen to be more sensitive and robust. Simultaneous NV-based temperature measurements on the NDs showed no substantial change in temperature. This further indicates that such quenching effects are not a result of the heating of the NDs.

30-3: Quantum Sensing of Temperature Increase Due to Thermoplasmonic Effects Using Fluorescent Nanodiamonds (Oral)
Start Time: 12:00 PM (15 Mins)
Speaker/Author: Eklavy Vashist (INDIAN INSTITUTE OF SCIENCE, India); Souvik Ghosh and Ambarish Ghosh (Indian Institute of Science, India)
Presenter: Eklavy Vashist

Abstract: In addition to the nanoscale electric field enhancement in plasmonic structures, there is an increase in the local temperature at the nanoparticle surface due to light absorption at resonance, resulting in Thermoplasmonics effects. Therefore, understanding and quantifying the local heating and resultant effects with nanoscale spatial resolution is crucial for engineering plasmonic devices for various applications. Here we report plasmonic heating of Au nanoparticles using a resonant light illumination and an estimation of associated temperature rise using Nitrogen-Vacancy (NV) centers in nanodiamonds (NDs). A custom-built wide field measurement setup detects and analyses the modulation of fluorescence spectra from the NDs close to the plasmonic hotspots. The plasmonic resonance absorption in Au nanoparticles and associated local heating is also studied using COMSOL Multiphysics which matches closely with our experimental results and validates our measurement system. This setup allows to make a thermal map of the system without being limited by diffraction and can be extended to other systems.

30-4: Developing a research foundry for quantum systems (Invited Talk)
Start Time: 12:15 PM (30 Mins)
Speaker/Author: Prof. Manas Mukherjee, Institute of Material Research and Engineering, A*star and Centre for Quantum Technologies, NUS, Singapore
Presenter: Prof. Manas Mukherjee

Abstract: Quantum technologies in general and quantum computing (QC) in particular is predicted to be one of the most disrupting among the emerging technologies. Therefore translation of this technology is happening at a neck break speed. As an example, small scale quantum computers are now available as software as a service (SaaS) offered by leading corporates as well as startups. Even though the current backend quantum hardware are too noisy to yield any useful quantum advantage, they are the best playground to explore the potential of quantum computers. Given the complexity of developing a full stack QC, it is essential to develop a library of quantum devices. At the National Quantum Foundry, we develop superconducting circuit chips along with integrated ion traps, photonics circuits and Si-donor qubits.

30-5: Technologies for next generation Quantum Computing (Sponsored)
Start Time: 12:45 PM (15 Mins)
Speaker/Author: Mr. Mandar Kumthekar, Oxford, NanoScience
Presenter: Mr. Mandar Kumthekar

Abstract: Quantum computing is a breakthrough for solving some complex computations. Leading qubit approaches—superconducting-based and spin-based qubits—require a millikelvin temperature range to operate devices and a high number of RF lines, especially superconducting cables with necessary attenuators and modularity in systems for building a fault-tolerant, scalable large-scale quantum computer.

Session No: 31 | Session Title: Nitride based optical sources
Audi: 9 | 11:15 AM-01:00 PM | **Session Chair:** Prof. Sudharsanan Srinivasan
Track: LED & Semiconductor Lasers: Device, Physics & Modules (LL)
Date: 13-Dec-22

31-1: Progress in Growth and Fabrication of AlGaN LEDs on SiC Substrates (Invited Talk)
Start Time: 11:15 AM (30 Mins)

Speaker/Author: Prof. Burhan SaifAddin, King Fahd University of Petroleum and Minerals, Saudi Arabia
Presenter: Prof. Burhan SaifAddin

Abstract: The disinfection industry would greatly benefit from efficient high-power deep-ultraviolet light-emitting diodes (UV-C LEDs). In this talk, I discuss progress in the growth and fabrication of AlGaN LEDs on SiC Substrates. First, we will discuss the physics of lighting with double heterostructures LEDs and the physics of nitride semiconductors. Then I will discuss the development of epitaxial growth and processing techniques for the best demonstration of UV LEDs (260—275 nm) on SiC substrate, which was enabled by novel thin-film flip-chip processes and resulted in high LED light extraction efficiency relative to planner sapphire or AlN substrates. Moreover, I will discuss tunnel junction UV LEDs and how they can significantly improve LED performance and the potential of UV disinfection.

31-2: Design and Performance Analysis of Electron Blocking Layer Free GaN/AlInN/GaN Nanowire Deep-Ultraviolet LED (Oral)
Start Time: 11:45 AM (15 Mins)
Speaker/Author: Samadrita Das and Trupti Ranjan Lenka (National Institute of Technology Silchar, India); Fazal Talukdar (NIT Silchar, India); Giovanni Crupi (University of Messina, Italy); Hieu Nguyen (New Jersey Institute of Technology Newark, USA)
Presenter: Samadrita Das

Abstract: We report on the illustration of the novel electron blocking layer (EBL) free AlInN nanowire light-emitting diodes (LED) with a single-quantum well (SQW) operating in the deep ultraviolet (DUV) wavelength region (sub-250 nm). We have systematically analyzed the results using Atlas TCAD and compared them with simulated AlGaN nanowire DUV LED. From the simulation results, a significant efficiency droop was observed in AlGaN LED, attributed to the significant electron leakage. However, compared to AlGaN nanowire DUV LED at a similar emission wavelength, the proposed (SQW) AlInN-based light-emitter offers higher internal quantum efficiency without droop up to the current density of 1500 A/cm2 and high output optical power. Further research shows that the performance of the AlInN DUV nanowire LED reduces with multiple QWs in the active region due to the presence of the non-uniform carrier distribution in the active region. This study provides important insights into the design of a new type of high-performance AlInN nanowire DUV LED, by replacing currently used AlGaN semiconductors.

31-3: Improved Carrier Confinement With Engineered Electron Blocking Layer in InGaN/GaN-Based Micro-LED at a Lower Current Density (Oral)
Start Time: 12:00 PM (15 Mins)
Speaker/Author: Chandra Prakash Singh (IIT Jammu North Block National Highway 44, India); Kankat Ghosh (IIT Jammu, India)
Presenter: Chandra Prakash Singh

Abstract: An engineered electron blocking layer structure has been proposed to alleviate the significant electron leakage problem in InGaN/GaN multiple quantum well based micro-LED at lower current density (@ 1A/cm 2). The simulation results show that the level of electron concentration leakage in the p-region is drastically reduced by ~10 16 times compared to a reference structure (Sample A), added with improved hole injection efficiency @ 1 A/cm 2 . As a result, the internal quantum efficiency is enhanced by ~1.4 times with a 50% reduction in input operating voltage compared to Sample A to reach 1 A/cm 2 . In addition, the efficiency droop in our proposed structure is reduced from 45% to 10% @ 200 A/cm 2 compared to Sample A.

31-4: Engineering of p-AlxGa1-xN Layer in AlGaN-Based UV-C LED to Improve Efficiency Droop by ~83% and IQE by ~41% (Oral)
Start Time: 12:15 PM (15 Mins)
Speaker/Author: Balkrishna Choubey (Indian Institute of Technology Jammu, India); Kankat Ghosh (IIT Jammu, India)
Presenter: Balkrishna Choubey

Abstract: In this simulation, we have investigated the engineering of p-AlxGa1-xN layer to improve the internal quantum efficiency (IQE) and efficiency droop of AlGaN-based ultraviolet-C light emitting diodes. This leads to enhancement of the carrier injection and the radiative recombination (RR) rate of the proposed structure. Linear grading of p-AlxGa1-xN layer reduces the carrier spill-off from the active region by increasing the potential barrier height for electrons (from 242.71 meV to 313.32 meV) in the conduction band. Meanwhile, it also improves the hole injection by reducing the potential barrier height for holes (from 443.7 meV to 384.7 meV) in

the valence band. The reduction in the internal electric field of the multiple quantum wells (from 62.4 eV/μm to 52.9 eV/μm) confirms the reduction of quantum confined stark effect (QCSE) in the engineered sample. The reduction of QCSE and the enhancement of hole injection increases the RR rate by ~10 fold for the quantum wells in the engineered sample compared to the control sample, hence increasing the IQE by ~41%. Also, the efficiency droop is improved by ~83%. The Al-composition of p-AlxGa1-xN layer was so adjusted that both the control and engineered samples emit at same wavelength, i.e., ~276 nm.

31-5: III-Nitride Nanowire LEDs for Enhanced Light Technology (Invited Talk)
Start Time: 12:30 PM (30 Mins)
Speaker/Author: Prof. Trupti Ranjan Lenka, National Institute of Technology Silchar, India
Presenter: Prof. Trupti Ranjan Lenka

Abstract: In this talk, the prospects of III-nitride nanowire based LEDs for enhanced luminescence are presented. It comprises of design, modelling and simulation of novel nanowire LED structures. The electron blocking layer and multiple quantum wells are introduced for enhanced light. A novel, white LED with improved thermal characteristics is designed and simulated for providing efficient light which may be used in underground mining. The LED is designed with HfO2/SiO2 doped silicon layer as encapsulation material which results 30.1% enhanced efficiency with minimization of electrons overflow. The encapsulate material based on nano HfO2/SiO2 not only enhances light extraction but also opens a broad new range of encapsulate engineering capabilities.

Session No: 32 | Session Title: Advances in Silicon Based Power Devices
Audi: 10 | 11:15 AM-01:00 PM | **Session Chair:** Dr. Ritu Sodhi
Track: Advanced Power Device Technology (APDT)
Date: 13-Dec-22

32-1: Advances in Silicon Power Semiconductor Devices (Invited Talk)
Start Time: 11:15 AM (30 Mins)
Speaker/Author: Dr. Madhur Bobde, Alpha & Omega Semiconductor
Presenter: Dr. Madhur Bobde

Abstract: Silicon power MOSFETs have made tremendous advancements in the past decade. The key concept that has led to this is that of charge balance. In conventional power MOSFET device the maximum doping level and the thickness of the drift region is limited by blocking voltage constraints and a triangular electric field results in its sub-optimal utilization. The concept of charge balance involves adding an opposite polarity of charge in the drift region compared to default doping to modify the shape of electric field from triangular to trapezoidal for better utilization of drift region for voltage blocking, and allow significantly higher doping concentration for lower conduction losses. For low voltages (below 400V) the popular device structure to achieve this is the Split Gate Transistor (SGT). This device utilizes trench MOS charge balance with a shield electrode under the gate. In addition to significantly improving the On Resistance per unit area (~3x for 100V blocking), the shield electrode also significantly reduced the gate to drain miller capacitance (Crss) and Crss/Ciss ratio to allow for high frequency switching. For high voltages above 400V, the depth of trench and thickness of liner oxide make SGT device impractical to fabricate. As a result, the Super-Junction transistor has emerged as the most successful MOSFET for high voltages. This device utilizes alternating P and N columns in the drift region thereby creating a charge balance. Methods such as multi epi, deep trench and fill have been demonstrated and are commercially successful for making superjunction transistors. These can achieve an On-Resistance reduction of up to 8x compared to planar DMOS transistor. However, presence of alternating P and N columns also results in peculiar Capacitance curves, particularly the Crss which drops sharply at low drain biases and then increases at higher drain biases. It also exhibits snappy diode reverse recovery. Charge balanced structure is also finding use in bipolar devices such as IGBT and Fast recovery diodes. In these devices, charge balance is used for various performance enhancements such as improving turn-off losses, injection enhancement, and controlling injection efficiency for faster switching. The goal of this seminar is to understand the device physics and electrical characteristics of charge balanced devices in unipolar and bipolar power devices. This seminar is intended for intermediate level audience.

32-2: Recent Progress of scaled Si-IGBT and related technologies (Invited Talk)
Start Time: 11:45 AM (30 Mins)
Speaker/Author: Prof. Shin-ichi NISHIZAWA, Kyushu University, Japan
Presenter: Prof. Shin-ichi NISHIZAWA

Abstract: For the future power devices, Si-IGBT is still under improvement. To achieve more high power densities, size reduction, etc., there are many researches related to Si wafer, device processes, device structures, etc. are ongoing. In this presentation, the scaled Si-IGBT as the future advanced Si-IGBT, and related wafer, processes technologies are explained.

32-3: Recent progress in the trench Clustered IGBT (Invited Talk)
Start Time: 12:15 PM (30 Mins)
Speaker/Author: Prof. Shankar Ekkanath Madathil, University of Sheffield
Presenter: Prof. Shankar Ekkanath Madathil

Abstract: Significant progress has been achieved in IGBTs in recent years. However, further improvements in on-state performance, switching frequency and long-term reliability are becoming difficult to realize due to the Dynamic Avalanche (DA), which limits the high current density operation capability. DA free operation can enable reduction in the gate resistance to reduce switching losses and enhance reliability. The Trench Clustered IGBT (TCIGBT) is the only DA free solution that has been experimentally proven so far. Its self-clamping feature and PMOS operation are effective to manage the peak electric field distribution beneath trench gates. In addition, the inherent thyristor operation offers much lower on-state losses even when comparing the NPT-TCIGBT to the FS-IGBT. In this paper, recent results of the 1.2 kV TCIGBT in field-stop technology is reported. A low on-state voltage drop of 1.5 V is achieved at room temperature. The saturation current levels are effectively controlled by the self-clamping feature. Moreover, experimental results confirm that the fabricated devices exhibit dynamic avalanche free switching performance as well as high dV/dt controllability.

32-4: Inverted SOA and Transient Non-Linearity of LDMOS Devices With RESURF-Implant (Oral)
Start Time: 12:45 PM (15 Mins)
Speaker/Author: Aakanksha Mishra (Indian Institute of Technology Delhi, India); Sampath Kumar Boeila (Indian Institute of Science, India); Avinash Kumar Singh, Shubhank Gupta and M. Monish Murali (Indian Institute of Science Bangalore, India); Amit Kumar Singh (Semi-Conductor Laboratory Mohali, India); Ankur Gupta (Indian Institute of Technology Delhi, India); Mayank Shrivastava (Indian Institute of Science Bangalore, India)
Presenter: Aakanksha Mishra

Abstract: Reduced surface field (RESURF) technique in the laterally double-diffused MOS (LDMOS) devices offers a promising solution of high voltage alternative over conventional LDMOS devices with improved figure of merits. This paper addresses the safe operating area (SOA) concerns and ON-state breakdown driven limitations of RESURF technique, highlighting the inverted SOA behavior. Using electrothermal simulations on TCAD tool, this work also investigates the influence of RESURF-implant on the lattice heating in the LDMOS devices.

Session No: 33 | Session Title: Process Integration and Technology

Audi: 11 | 11:15 AM-01:15 PM | **Session Chair:** Prof. Deleep Nair
Track: Advanced Logic Technologies (ALT)
Date: 13-Dec-22

33-1: Process integration of CMOS technologies, from planar to FinFET (Invited Talk)
Start Time: 11:15 AM (30 Mins)
Speaker/Author: Dr. Victor Chan, IBM Research
Presenter: Dr. Victor Chan

Abstract: In this talk, the challenge and limitation of CMOS scaling will be discussed.
CMOS Scaling has been driven by process integration of new architecture and materials. Continuously scaling and technology innovations, with focus on Front-End-of-Line (FEOL) and Middle-of-Line (MOL) processes, were enabled in the last two decades. Strain engineering and better gate oxide have been improved in early stage to increase device performance, lower supply voltage and leakage. Device architecture from planar to FinFET transistors increases effective width in a given device footprint starting from 14nm technologies. Optimizing Fin material to enhance channel mobility is a challenge. In addition, improving gate to contact pitch over fins and lowering contact resistance are necessary.

33-2: Atomic Layer Deposition (ALD): An essential process for advanced semiconductor technologies (Invited Talk)
Start Time: 11:45 AM (30 Mins)
Speaker/Author: Dr. Vamsi K. Paruchuri, ASM International N.V., Netherlands

Presenter: Dr. Vamsi K. Paruchuri

Abstract: As the semiconductor industry has adopted increasingly more complex materials, architectures and 3D geometries with critical dimensions in the nanoscale range, atomic layer deposition (ALD) has become essential for enabling those inflections and driving the semiconductor industry forward. This presentation will provide an overview of ALD process and the critical role it played in some of the inflections over the past two decades such as high-k metal gate, FinFET, and 3D-NAND technologies. It will also provide some insights into how ALD will play an even more significant role in technologies of the future such as gate all around (GAA) and complementary FET for logic, and 3D-DRAM, novel emerging memory technologies.

33-3: A Journey through the wild west of lithography capability spanning the last three decades (Invited Talk)
Start Time: 12:15 PM (30 Mins)
Speaker/Author: Dr. Anton deVilliers, Tokyo Electron Limited (TEL), USA
Presenter: Dr. Anton deVilliers

Abstract: Over the last 20years or so the industry scale path has seen many transitions to enable what each preceding generation of technology thought was impossible. New technology becomes possible with the addition of patterning techniques that help enable each generation of smaller designs. This talk will go through some of the enabling technologies and how the industry of chip making made breakthrough after breakthrough to truly enable parts to be printed at dimensions and geometries far more exotic than any could have imagined. We will take a look at the recent history of technology scaling enablers and how they shaped the industries roadmaps and understanding of scaling.

33-4: Dry Etch Challenges and Solutions for FinFET Technology and Beyond (Invited Talk)
Start Time: 12:45 PM (30 Mins)
Speaker/Author: Dr. Ganesh Upadhyaya, LAM Research
Presenter: Dr. Ganesh Upadhyaya

Abstract: The semiconductor industry has migrated from planar to FinFET technology during the past 10 years. Soon the industry will transition to gate-all-around architecture thereby introducing yet another major technological inflection. Patterns created by lithography, and film stack created by deposition need to be carefully shaped by dry etch to form the desired transistor structures. Etch complexity has increased node over node and has required the development of cutting edge equipment to meet the tight tolerances imposed by device requirements. This talk will provide an overview of dry etch innovations from Lam Research to address challenges for the FinFET era and beyond.

Session No: 34 | Session Title: Fundamentals of 2D devices 2
Audi: 1 | 02:30 PM-04:15 PM | **Session Chair:** Prof. Eilam Yalon
Track: 2D Material Based Technologies (2DT)
Date: 13-Dec-22

34-1: Emerging 2-D Material Beyond MoS2: From Fundamental Physics to Applications (Invited Talk)
Start Time: 02:30 PM (30 Mins)
Speaker/Author: Dr. Brajesh Rawat, Indian Institute of Technlogy Ropar Rupnagar, Punjab, India
Presenter: Dr. Brajesh Rawat

Abstract: The demand for lower power consumption and higher integration density in the electronic system has become the main driving force of the industry's search for devices based on novel 2-D materials. In this talk, I will discuss electronic devices based on emerging two-dimensional materials, such as MoS2, BP, AS2, InSe, GeTe, Ti2S, ReS2, using a multi-scale modeling methodology based on the non-equilibrium Green's function approach. I will focus on investigating performance limits and advantages of novel 2-D materials for both digital and analog applications with major attention to their performance benefits over silicon counterparts. Further, I will discuss the use of the two-dimensional material channel for multigate devices and provide our perspectives on future developments.

34-2: Unique Reliability Concern on Intrinsic MoSe2 FET Channel (Oral)
Start Time: 03:00 PM (15 Mins)
Speaker/Author: Utpreksh Patbhaje and Rupali Verma (Indian Institute of Science, India); Mayank Shrivastava (Indian Institute of Science Bangalore, India)
Presenter: Utpreksh Patbhaje

Abstract: MoSe2 is one of the ambipolar 2D material that provides a lucrative option going forward towards sub-μm channel length scales for transistor application. Impact of long time and high field operational effects due to channel and contacts of MoSe2 FETs are analyzed in this work to understand the concerning reliability factors due to evolution of channel and contacts. In this work, we investigate a unique operational scenario to isolate the effects of channel and contact interface by stressing MoSe2 devices in floating gate condition to minimize the contribution of trap states provided by the oxide. Channel and contact states provide competing mechanism to determine performance deviations which should be better understood going forward.

34-3: Plasma and Pulse Stress Combined Flawless Effect for Performance Boosting of MoS2 FETs (Oral)
Start Time: 03:15 PM (15 Mins)
Speaker/Author: Anand Kumar Rai and Mayank Shrivastava (Indian Institute of Science Bangalore, India)
Presenter: Anand Kumar Rai

Abstract: Schottky contact is still a bottleneck for MoS2- based FETs, caused by fermi level (FL) pinning, leading to low drive current in 2D TMD-based FETs. The primary reasons for FL pinning are metal induced gap states (MIGS) and nonuniformity on MoS2 surfaces like sulfur vacancies. Here we propose a method, which can enhance the overall characteristics of MoS2 FETs including drive current. On MoS2 flakes, a 5 sec CF4 plasma treatment of 18 W RF power was used after fully developing the contact region, post which Ni/Au contact deposition was done. During characterization of FETs, a series of pulses were applied across source(S)-drain(D) terminal in floating gate condition. After application of pulses, the ION gets improved by 55 μA/μm after 20 pulses, and by 75 μA/μm after 200 pulses. The contact resistance (Rc) also gets reduced from 12.55 KΩ-μm to 1.74 KΩ-μm after the application of 200 such pulses. Similarly, mobility and subthreshold swing also get improved. With continuous pulsing across S/D terminal of the FET, whose contact was treated using plasma, n-type doping in the channel was observed and confirmed using Raman and PL spectroscopy. The combined effect of n-type doping in the channel and reduced contact resistance, results in overall performance boosting of MoS2 FET.

34-4: Impact Ionization of Excitons by In-Plane Electric Field Accelerated Hot Carriers in Monolayer WS2 (Oral)
Start Time: 03:30 PM (15 Mins)
Speaker/Author: Rupali Verma, Utpreksh Patbhaje and Asif Altaf Shah (Indian Institute of Science, India); Mayank Shrivastava (Indian Institute of Science Bangalore, India)
Presenter: Rupali Verma

Abstract: Monolayer TMDs are projected for future optoelectronic technologies attributed to their direct bandgap, which ensures efficient light absorption in the monolayer limit, suited for flexible and transparent photo-sensing and photo-emitting applications. By analyzing the variation in the photoluminescence (PL) spectrum and through in-situ photocurrent measurement with increasing in-plane electric field, it is observed that in a metal-semiconductor-metal photodiode with transparent and flexible monolayer WS2 as the photoactive material, the impact ionization of low binding energy charged biexcitons and trions at low temperature and the impact ionization of trions at room temperature contributes to the photocurrent in the device, unlike the ionization of neutral excitons in conventional semiconductors. Also, the impact ionization (or delocalization) of localized excitons by emission of a trap state is observed at low temperature (~ 12 K) due to scattering by in-plane field accelerated free carriers. The effect is manifested as the quenching of the localized exciton emission in the observed photoluminescence at high lateral fields. An enhancement in the free exciton emission is observed with increasing bias.

34-5: Interlayer transport and defect density of states in MoS2 flakes (Invited Talk)
Start Time: 03:45 PM (30 Mins)
Speaker/Author: Prof. Yashowanta N Mohapatra, IIT Kanpur
Presenter: Prof. Yashowanta N Mohapatra

Abstract: There is a concerted effort to develop functional inks of 2D materials to realize printable electronic devices using them and MoS2 is principal among them. The material for formulation of ink is derived from flakes through different strategies. There is a need though to correlate the transport parameters and defect density of states (DOS) in flakes in order to enable their traceability to functional inks and materials. I will first share our results on interlayer transport studies in an effort to understand underlying mechanisms. I will also discuss a convenient method of measuring defect DOS as a function of temperature in flakes of MoS2 to understand their origin. Then I will share our efforts at formulation of inks for MoS2 from materials of different origin.

Session No: 35 | Session Title: Ferroelectric, Negative Capacitance and Tunnel FET
Audi: 2 | 02:30 PM-04:15 PM | **Session Chair:** Prof. Pramod Tiwari
Track: Modelling and Simulations (MS)
Date: 13-Dec-22

35-1: Modeling, simulation and applications of engineered TFETs (Invited Talk)
Start Time: 02:30 PM (30 Mins)
Speaker/Author: Prof. SATYABRATA JIT, Indian Institute of Technology (BHU) Varanasi, INDIA
Presenter: Prof. SATYABRATA JIT

Abstract: The tunnel field effect transistor (TFET) has drawn considerable attentions for future generation low-power VLSI/ULSI applications due to its extremely low sub-threshold current and good switching characteristics. The TFET possesses low sub-threshold swing below the Boltzmann limit of 60 mV/decade of the bulk MOSFETs. However, the major drawback of the TFET is its very poor ON current. Several techniques have been introduced to improve the performance of the TFETs through various structural modifications. The present talk will introduce the performance analysis of some engineered TFET structures via theoretical modelling and commercially available TCAD simulations. Finally, some applications of the engineered TFETs in the SRAM design and level-free bio-sensors will also be discussed.

35-2: On the Memory Window Variability in a 3-D Multi-Granular Ferroelectric FET Including Grain Boundaries (Oral)
Start Time: 03:00 PM (15 Mins)
Speaker/Author: Nilesh Pandey (Indian Institute of Technology Kanpur & Kanpur, India); Ashish Phogat and Yogesh Chauhan (Indian Institute of Technology Kanpur, India)
Presenter: Nilesh Pandey

Abstract: This paper analyzes the variability in the memory window of a ferroelectric FET induced by distinct grain patterns. The Poisson Voronoi algorithm nucleates the random grain texture in MATLAB, which is coupled with TCAD-Sentaurus to obtain the Id - Vg characteristics. The grain texture with boundaries exhibits larger variability than the grain texture without boundaries. The memory window decreases with the emergence of grain boundaries. Furthermore, a multi-grain pattern along the ferroelectric thickness direction is also incorporated in the study. The multi-granular ferroelectric layer possesses a higher variability than the mono-grain layer. Additionally, linearly increasing and decreasing polarization profiles are assumed in the ferroelectric grains, and such polarization distribution's impact on the memory window variability is analyzed. The random nucleation of grains in the ferroelectric layer establishes a replica of the experimental growth mechanism.

35-3: Ferroelectric Negative Capacitance Inspired Driver Circuits for Electrostatic MEMS Actuators (Oral)
Start Time: 03:15 PM (15 Mins)
Speaker/Author: Jeffin Shibu (Indian Institute of Technology Madras, India); Raghuram Tattamangalam Raman (GlobalFoundries, India); Abhilash O. S, Arun Kumar and Arvind Ajoy (Indian Institute of Technology Palakkad, India)
Presenter: Jeffin Shibu

Abstract: Electrostatic MEMS actuators require high operating voltages. It has been predicted that a ferroelectric negative capacitance connected in series with a MEMS actuator, forming a hybrid actuator, can reduce its operating voltage. We propose a driver circuit that mimics the behaviour of such hybrid actuators. Electrostatic actuators also suffer from pull-in instability, wherein the movable electrode snaps down to hit the bottom electrode beyond a certain applied voltage, called the pull-in voltage. Pull-in instability prohibits the use of entire air-gap for stable operation. We modify the proposed driver circuit to eliminate pull-in, resulting in full-gap travel. Using our topology, we illustrate both non-linear and linear quasi-static response for pull-in free operation. The results obtained using the numerical and circuit simulations and analytical predictions are in good agreement with each other. Thus, the proposed driver circuits can aid in the design of pull-in free electrostatic MEMS actuators.

35-4: Role of Negative Differential Resistance in Improving Analog Performance of Negative Capacitance FETs (Oral)
Start Time: 03:30 PM (15 Mins)
Speaker/Author: Anant Singhal and Yogendra Machhiwar (Indian Institute of Technology Jodhpur, India); Harshit Agarwal (Indian Institute of Technology Jodhpur, USA)
Presenter: Anant Singhal

Abstract: In this work, we discuss the prospects of a negative capacitance field effect transistor for analog applications. In common source amplifier configuration, NCFET evince improved voltage gain as compared to the baseline device. We show that negative differential resistance (NDR), which is undesirable for logic applications, plays a key role in gain enhancement. Other performance metrics like frequency response, cut-off frequency, transconductance efficiency etc. are also studied. Our study shows that NDR may be helpful in realizing short channel analog transistors. Intel's 20nm FinFET transistor is taken as a baseline device and TCAD simulation models are calibrated to match the input and output characteristics. Results of this work can be extended to advanced GAA nanosheet transistors based NCFETs.

35-5: Steep-Slope Technology for Continued Scaling: Prospective and Recent Developments (Invited Talk)
Start Time: 03:45 PM (30 Mins)
Speaker/Author: Prof. Harshit Agarwal, IIT Jodhpur
Presenter: Prof. Harshit Agarwal

Abstract: Steep-Slope technology is considered as a booster for high-performance AI and ML integrated circuits. Industry is actively looking beyond traditional CMOS devices as it is increasingly difficult to meet device level challenges posed by emerging AI, ML and IoT applications. This is largely due to the fact that such applications simultaneously require high performance, low power and high integration. ITRS 2.0 also lists SS technology as the only solution for power challenges. In this talk, we will discuss recent developments and challenges associated with the SS technology.

Session No: 36 | Session Title: Process Integration and Technology of Ga2O3 Devices

Audi: 3 | 02:30 PM-04:15 PM | **Session Chair:** Dr. Kamal Varadarajan
Track: Wide Bandgap Power Semiconductor Technologies (WPSD)
Date: 13-Dec-22

36-1: Diamond Electron Devices for Extreme Environment Electronics (Invited Talk)
Start Time: 02:30 PM (30 Mins)
Speaker/Author: Prof. Kaushik Nayak, Indian Institute of Technology Hyderabad
Presenter: Prof. Kaushik Nayak

Abstract: Diamond has emerged as a very promising ultra-wide bandgap (5.47 eV) elemental Gr - IV semiconductor material with characteristic high breakdown field, high thermal conductivity,
high electron and hole mobilities (μ_n: 4500 cm2/V · s and μ_p: 3800 cm2/V · s), and high saturation velocities (v_sat: 1 × 10^7 cm/s) for extreme environment, and high-power electronic applications.
In this talk we will discuss the background motivation and intuitive picture behind extreme environment physical characteristics, and their interaction with semiconductor devices. Here, we will briefly explore the need of wide-gap and ultra wide-gap semiconductor based devices for reliable and robust operations in extreme environments of space electronics, nuclear technologies and high-energy scientific instrumentation etc. Towards the end of the talk, we will discuss the key highlights of device modeling and simulation efforts to engineer and explore the devices physics of Diamond based unipolar electron devices (MOSFETs and Schottky Diodes) in LPER (Research Lab @ IITH) for extreme environment electronics.

36-2: Simulation Modeling of AlGaN/AlN/GaN Nano-HEMT on β-Ga2O3 Substrate for Emerging Terahertz Applications (Oral)
Start Time: 03:00 PM (15 Mins)
Speaker/Author: G. Purnachandra Rao and Nistha Baruah (National Institute of Technology Silchar Assam, India); Trupti Ranjan Lenka (National Institute of Technology Silchar, India); Rajan Singh (MLR Institute of Technology Hyderabad, India); Sharif Md. Sadaf (INRS University of Québec, Canada); Hieu Nguyen (New Jersey Institute of Technology Newark, USA)
Presenter: Trupti Ranjan Lenka

Abstract: This article reports a novel recessed gate AlGaN/AlN/GaN Nano-HEMT with field-plate on the β-Ga2O3 substrate. The simulation results show that the leakage current is drastically decreased due to the reduced lattice mismatch of the GaN layer with the substrate. It exhibited an electric field of 1.4MV/s, breakdowns at 72V, a current gain-cut-off frequency of 1.12THz and unilateral power gain-maximum oscillation frequency of 1.132THz, and a JFOM of 72.072 THz-V. Therefore, with the help of β-Ga2O3 as a substrate, the proposed novel HEMT exhibited terahertz frequency characteristics and superior JFOM value. Our results will pave the way for future high-frequency devices on β-Ga2O3 substrates.

36-3: Alternating Magnetic Field Hall Measurement on Low Mobility β-Ga2O3 Thin Film (Oral)
Start Time: 03:15 PM (15 Mins)
Speaker/Author: Soumen Kundu (Indian Institute of Science, Bangalore, India); Mahek Mehta (Indian Institute of Science Bangalore, India); Narasimhan K L (Indain Institute of Science, India); Sushobhan Avasthi (Indian Institute of Science & Centre for Nano Science and Engineering (CeNSE), India)
Presenter: Soumen Kundu

Abstract: In this paper we compare the conventional DC Hall technique and alternating magnetic-field Hall measurement on a 1% Si-doped β-Ga2O3 film. Such samples have a low carrier mobility, so accurately measuring the Hall voltage is quite challenging. To obtain a measurable signal with the Werner's DC Hall technique, one needs high magnetic-field of 1.5 T. Even then, the true Hall signal (V Hall) is 22 times lower than the misalignment voltage. On the other hand, with the Alternating magnetic-field Hall technique even low mobility values can be measured with a magnetic-field of just 0.2 T, without any interference from misalignment voltage. The alternating magnetic-field does produce a Faraday voltage, which is the same order of magnitude as the AC Hall signal. However, the Faraday component does not vary with the applied voltage. Also, the Faraday component can be scale down using low frequency and reducing the effective loop area. The AC Hall setup gives an opportunity to characterize transport in thin films with mobility less than 1 cm2 /Vs.

36-4: Effect of HF Surface Treatment on Electrical Properties of β - Ga2O3 Schottky Barrier Diodes (Oral)
Start Time: 03:30 PM (15 Mins)
Speaker/Author: Pooja Sharma and Saurabh Lodha (Indian Institute of Technology Bombay, India)
Presenter: Pooja Sharma

Abstract: β – Ga2O3 Schottky barrier diodes were fabricated on Sn-doped n – Ga2O3 ($\bar{2}01$) substrates to quantify the effect of HF solution treatment on their electrical properties. A 0.2 eV increase in Schottky barrier height resulting in ~ 40 V enhancement in reverse breakdown voltage has been demonstrated for the devices fabricated on a substrate treated with HF solution as compared to diodes on an un-treated surface. The increase in breakdown voltage does not compromise the on-resistance of the diodes. The devices showed excellent current-voltage characteristics with near unity ideality factors and high on-off current ratio.

36-5: Role of Sub-oxides in LPCVD of β-Ga2O3 (Invited Talk)
Start Time: 03:45 PM (30 Mins)
Speaker/Author: Dr. Amit Verma, Indian Institute of Technology Kanpur, India
Presenter: Dr. Amit Verma

Abstract: β-Ga2O3 is an ultra-wide bandgap semiconductor which is quite promising for high-power device applications due to its high breakdown electric field of ~7-8 MV/cm and availability of melt-grown bulk substrates. Several epitaxial techniques have been explored for thin film growth of this material. Among these techniques, low pressure chemical vapour deposition (LPCVD) is quite promising due to its high growth rates, good material quality, and controlled doping capability. In this talk, the current status of β-Ga2O3 LPCVD will be presented along with some new experimental results which highlight the importance of suboxide formation and desorption during LPCVD of β-Ga2O3.

Session No: 37 | Session Title: Electrochemical Sensors
Audi: 4 | 02:30 PM-04:15 PM | **Session Chair:** Prof. Sushmee Badhulika
Track: Sensors and Bio-Electronics (SBE)
Date: 13-Dec-22

37-1: Studies on NO2 gas detection using IGZO-based chemoresistive sensors (Invited Talk)
Start Time: 02:30 PM (30 Mins)
Speaker/Author: Prof. Sunil Babu Eadi, Chungnam National University, South Korea
Presenter: Prof. Sunil Babu Eadi

Abstract: The development of a high-response, stable and reliable NO2 sensor is need of hour. Indium-Gallium-Zinc Oxide (IGZO), one of many chemoresistive materials, has recently emerged as the best choice due to its unique characteristics such as, high electron mobility (10–100 cm2/(Vs), porous amorphous state, and low growth temperature. This unique properties makes IGZO as a superior candidate for gas detection application. Therefore, to develop high response NO2 gas sensor, this studies focuses on investigation of IGZO thin films sensors under various growth conditions and annealing processes. Thermal annealing techniques such as different ambient, temperature and pressure were systematically explored.

37-2: Green Synthesized CaO NPs Based Electrochemical Sensor for the Sensitive Detection of Dopamine (Oral)
Start Time: 03:00 PM (15 Mins)
Speaker/Author: T S Sunil Kumar Naik and Simranjeet Singh (Indian Institute of Science, India); Pavithra N (INDIAN INSTITUTE OF SCIENCE, India); Radhika Varshney (Indian Institute of Science, Bangalore, India); Praveen C Ramamurthy (Indian Institute of Science, India)
Presenter: T S Sunil Kumar Naik

Abstract: Here, a novel approach for synthesising calcium oxide (CaO) from seashells was carried out and used as a sensor material for detecting dopamine (DA). The existence of the CaO nanoparticle was confirmed by various characterization techniques like FTIR, UV-visible, and, XRD. The cyclic voltammetry (CV) method was employed for the analysis of DA using a carbon paste electrode (CPE) as the working electrode. The fabricated CaO-modified CPE (CaO/MCPE) was effectively used for the detection of DA using phosphate buffer saline (PBS) as a supporting electrolyte. The sensor exhibited excellent catalytic behavior for the detection of DA in the lower detection range (LLOD= 0.27 μM). Also, the practical application of the sensor was investigated.

37-3: Layer by Layer Self-Assembled MoS2-ZnO Heterostructure for Near Room Temperature NO2 Gas Sensor (Oral)
Start Time: 03:15 PM (15 Mins)
Speaker/Author: Rahul Gond and Prajjwal Shukla (Indian Institute of Technology Ropar, India); Mayank Baghoria and Bhanu Prakash (Institute of Nano Science and Technology, India); Brajesh Rawat (IIT Ropar, India)
Presenter: Rahul Gond

Abstract: Due to their excellent chemical and electronic properties, two-dimensional MoS 2 has emerged as a viable candidate for developing room temperature NO 2 sensors. However, the MoS 2-based gas sensor suffers from low sensitivity and incomplete recovery. Therefore, in this work, we fabricate and characterize layer-by-layer self-assembled MoS 2-ZnO heterostructure for near-room temperature NO 2 gas sensor. The results reveal that MoS 2-ZnO heterostructure exhibits high response and complete recovery for NO 2 gas with the excellent cross-sensitivity against CO, CO 2, NH 3 and SO 2 gases. Moreover, the long-term durability of the sensor is evident from the stable response curves even after 15 days. Further, the MoS 2-ZnO heterostructure sensor exhibits the room temperature response and recovery times of around 2.1 min. and 27.9 min., respectively, for 50 ppm NO 2 gas with the lowest detection limit of about 1 ppm.

37-4: Optimisation of Techniques for Fabrication of Nanopatterned Substrates (Oral)
Start Time: 03:30 PM (15 Mins)
Speaker/Author: Gouri Patil, Reshma Vasantha Ramachandran and Ambarish Ghosh (Indian Institute of Science, India)
Presenter: Reshma Vasantha Ramachandran

Abstract: Nanopatterned substrates have wide-ranging applications in fields stretching from the semiconductor industry to biomaterials. To improve the performance of these end-products, there is a need for scalable fabrication methods for these substrates with due consideration to their uniformity, yield and miniaturization. Here, we consider these substrates as seed layers on which nanomotors can be grown by glancing angle deposition. We discuss the requirements and consequent optimization of various methods and especially a soft lithography technique, which gives optimal outcomes.

37-5: Revisiting doping mechanisms in a mixed electronic-ionic conductor PEDOT:PSS (Invited Talk)
Start Time: 03:45 PM (30 Mins)
Speaker/Author: Prof. Merlyne De Souza, The University of Sheffield
Presenter: Prof. Merlyne De Souza
Abstract: The mechanism of doping and de-doping in conjugated polymers such as PEDOT:PSS has been widely discussed on account of their application in bioelectronics from electrochemical batteries/supercapacitors to neural electrodes and transducers. In a conventional theory, there are three expected mechanisms of doping (i) Capacitive, leading to box shaped CV characteristics, whereby electrical double layers are formed at the surface of the polymer and the counter-electrode. This type of a film shows a capacitance independent of thickness. (ii) Faradaic, in which under positive bias, holes move towards the counter-electrode and react with species in the electrolyte leading to redox peaks in the cyclic voltammetry and (iii) Volumetric electrochemical doping, which

is a combination of the above two, caused largely by cation injection into the bulk of the film, leading to electronic-ionic coupling of the holes and cations [1-3].
We demonstrate that the doping mechanism of K+ in PEDOT:PSS is more complex than these simple scenarios. Our films are able to retain more ions in a Faradaic reaction than via purely capacitive doping, pointing to coupling between the sulfonate anion and cation.
References:-
1.Exploiting mixed conducting polymers in organic and bioelectronic devices, Scott Keene et al Phys. Chem. Chem. Phys., 2022, 24, 19144
2. Understanding Volumetric Capacitance in Conducting Polymers, Christopher M Procter et al, Journal of Polymer Science, Part B: Polymer Physics 2016, 54, 1433-1436.
3. Berggren, M., Malliaras, G. G., (2019), How conducting polymer electrodes operate, Science, 364(6437), 233-234. https://doi.org/10.1126/science.aaw9295.

Session No: 38 | Session Title: Thin Film Transistors
Audi: 5 | 02:30 PM-04:15 PM | **Session Chair:** Prof. Sanjiv Sambandan
Track: Macroelectronics & Displays: Devices, Circuits & Systems (DIS)
Date: 13-Dec-22

38-1: Ion conducting metal oxide and its application as gate dielectric of a low operating voltage thin film transistor (Invited Talk)
Start Time: 02:30 PM (30 Mins)
Speaker/Author: Dr. Bhola Nath Pal, Indian Institute of Technology (BHU)
Presenter: Dr. Bhola Nath Pal

Abstract: A thin film of ion-conducting metal oxide (ICMO) contains mobile light ions like Li+, Na+, K+ which originates a high areal capacitance of the film due their ionic polarization. An insulating ICMO has low DC conductivity with high AC conductivity which is suitable for using it as a gate dielectric of a low operating voltage thin film transistor (TFT). In the last decade a significant achievement has been made on solution processed ICMO based metal oxide TFT which can attain a carrier mobility > 20 cm2/Vs with an on/off ratio >105 under 2 V operating voltage. This presentation will focus on the development of these solution processed ICMOs for low operating voltage metal oxide TFT fabrication and its various applications including phototransistor, memory transistor and synaptic transistor.

38-2: Fully printed, ultra-flexible and low temperature processed oxide electronics (Invited Talk)
Start Time: 03:00 PM (30 Mins)
Speaker/Author: Prof. Subho Dasgupta, Indian Institute of Science, India
Presenter: Prof. Subho Dasgupta
Abstract: Research on printed electronics was initiated with the invention of easy-to-print organic semiconductors in the last century, whereas, it is only about a decade now that printed oxide semiconductors and devices have come up as a possible competitor to this well-matured organic electronics activity. Here, the oxygen deficient n-type oxides can demonstrate carrier mobility close to polycrystalline silicon, and maintain their band transport even when amorphous in nature. In fact, today the dc performance of these solution-processed oxide thin film transistors (TFTs) is no way inferior to their physical vapor deposited counterparts. However, the limited printing resolution has always posed a major hindrance to achieve high operation frequency. In addition, oxides are often criticized for their high process temperatures, and lack of mechanical flexibility. Unsurprisingly, the ceramic oxides are inherently brittle and demonstrate very little (typically <1%) strain tolerance. In contrast, here in this presentation a couple of novel material and (device) design strategies will be discussed that helps to achieve significantly large (up to 5%) strain tolerance under dynamic mechanical test conditions. At the same time, high frequency operation from several tens of kHz to hundreds of kHz will be demonstrated.

38-3: Inkjet-Printed Mesoporous Indium Oxide-Based Near-Vertical Transport Thin Film Transistors and Pseudo-CMOS Inverters (Oral)
Start Time: 03:30 PM (15 Mins)
Speaker/Author: Nehru Devabharathi and Jyoti Ranjan Pradhan (Indian Institute of Science, India); Subho Dasgupta (Indian Institute of Science (IISc), Bangalore, India)
Presenter: Jyoti Ranjan Pradhan

Abstract: Oxide semiconductors are increasingly becoming the material of choice in the emerging printed and flexible electronics domain. While they have attracted tremendous research attention in the area of solution processed/printed electronics, the vacuum deposited amorphous oxide semiconductor TFTs have also achieved

serious commercial success in the transparent and curved display industries. Nonetheless, it may be noted that although the n-type oxides demonstrate excellent electronic transport, the performance of the hole conducting p-type oxides are still unsatisfactory and thus it affects the fabrication of all oxide complementary metal oxide semiconductor (CMOS) circuits. In order to resolve the issue, unipolar depletion-load type pseudo-CMOS inverters have recently been proposed. In this regard, here, we demonstrate a co-continuous mesoporous indium oxide based thin film transistor (TFT) technology with edge-FET architecture and near vertical transport. At the next step, high performance, unipolar depletion-load type inverters have been fabricated using these edge-FET TFTs. The fabricated TFTs have shown average ON-current of 1.95 mA alongside excellent On/Off ratio (>10 7). On the other hand, the depletion-load type inverters have demonstrated sharp voltage transfer characteristics (VTC) with a maximum signal gain of 58 at VDD= 2 V, supply voltage.

38-4: Scaling and device physics of amorphous oxide thin-film transistors (Invited Talk)
Start Time: 03:45 PM (30 Mins)
Speaker/Author: Prof. Ananth Dodabalapur, The University of Texas at Austin, USA
Presenter: Prof. Ananth Dodabalapur

Abstract: Thin-film transistor (TFTs) channel lengths need to shrink as performance requirements get more demanding for several applications. The switching speed and current drive capability are expected to improve as channel lengths reduce for most field-effect transistors. In many TFTs, contact resistance issues get severe at small channel length. Additionally, the physics of charge transport and basic performance characteristics can change quite substantially at small channel. We will review these properties for amorphous metal oxide TFTs with channel lengths in the range 50 nm – 5 micrometers. A new design for TFTs, based on the use of nanospike electrodes will be presented that greatly mitigates both the contact-resistance problem and short-channel effects as well as reduces DIBL and results in excellent sub-threshold and above threshold characteristics.

Session No: 39 | Session Title: Reliability Physics of Semiconductor Devices - 1
Audi: 6 | 02:30 PM-04:15 PM | **Session Chair:** Dr. Shubhakar (SUTD)
Track: Reliability Physics of Semiconductor Devices (RPSD)
Date: 13-Dec-22

39-1: Role of Defects on the Variability of STT-MRAMs and 3D CT NANDs (Invited Talk)
Start Time: 02:30 PM (30 Mins)
Speaker/Author: Dr. Md Zunaid Baten, Bangladesh University of Engineering and Technology (BUET), Bangladesh
Presenter: Dr. Md Zunaid Baten

Abstract: Spin-transfer torque magnetic RAMs (STT-MRAM) and three-dimensional (3D) charge-trapping (CT) NAND flash devices are considered to be highly prospective for next generation memory and neuromorphic applications owing to their small-footprints, scalability and compatibility with existing CMOS process technologies. Small dimensionalities, as well as inherently stochastic switching characteristics of STT-MRAMs, make these devices significantly prone to device-to-device and cycle-to-cycle variations. The stochastic nature of the charge capture/release processes associated with Program/Erase cycles of 3D CT-NANDs make these devices susceptible to device-to-device variabilities as well. In this work, based on experiments and simulations, the speaker will present recent results pertaining to the role of defects on the variability of memory and neuromorphic related performance metrics of STT-MRAMs and 3D CT NANDs.

39-2: Reliable STT-MRAM Technology for Advanced MCU & IOT Applications (Invited Talk)
Start Time: 03:00 PM (30 Mins)
Speaker/Author: Dr. Vinayak Bharat Naik, Technology Development, Globalfoundries, Singapore
Presenter: Dr. Vinayak Bharat Naik

Abstract: In the on-going era of artificial intelligence, IoT and autonomous vehicles, the semiconductor industry has actively been developing emerging non-volatile memory (NVM) technologies. Spin-Transfer-Torque magnetic random access memory (STT-MRAM) technology has proven to be a viable NVM technology solution to replace embedded flash in advanced microcontroller and microprocessor units. In this talk, the status of 22FDX® embedded MRAM technology for industrial-grade MCU & IOT applications, the crosstalk between MRAM & RF in a single EMI chip, and the trade-offs among MTJ device performances to optimize MRAM reliability for next-generation memory applications will be presented.

39-3: Role of Interfacial Oxide on Capacitance Matching in a Negative Capacitance FinFET: A Reliability Perspective (Oral)
Start Time: 03:30 PM (15 Mins)
Speaker/Author: Rajeewa Kumar Jaisawal (PDPM IIITDM Jabalpur, India); Sunil Rathore (PDPM-IIITDM & IEEE Member, India); Pravin Kondekar (PDPM IIITDM Jabalpur, Madhya Pradesh, India); Shashank Kumar Banchhor (Indian Institute of Technology Roorkee, India); Navjeet Bagga (PDPM IIITDM Jabalpur, India)
Presenter: Rajeewa Kumar Jaisawal

Abstract: Capacitance matching is a prime requirement to realize a Negative Capacitance (NC) FET. The ferroelectric (FE) layer in the gate stack with an interfacial oxide (IO) put forward two capacitances in series, resulting in internal voltage amplification when/if capacitance matching occurs. In recent NCFETs, we take doped-HfO2 as a FE layer and SiO2 as a conventional IO layer. However, different IO layers might offer different capacitances and thus require proper capacitance matching tuning. In this paper, using well-calibrated TCAD models, we realized a 14nm NC-FinFET and investigated the (i) impact of placing different IO layers on capacitance matching by keeping similar effective oxide thickness (EOT) and FE-layer (i.e., Si-doped HfO2) (ii) the overall impact of different IO layers on current ratio, subthreshold slope (SS), threshold voltage and analog metrics, such as gate capacitance, transconductance, output resistance, intrinsic gain, etc. (iii) impact of tuning the gate metal work-function on device characteristics. Thus, the proposed analysis is worth exploring as it provides the design guidelines for a reliable NC-FinFET operation.

39-4: HW/SW Codesign for Reliable Brain-inspired Computing on Unreliable Ferroelectric FET Technology (Invited Talk)
Start Time: 03:45 PM (30 Mins)
Speaker/Author: Prof. Hussam Amrouch, University of Stuttgart, Germany
Presenter: Prof. Hussam Amrouch

Abstract: In this talk, I will focus on the emerging ferroelectric technology and its great potential in building efficient in-memory computing architectures. I will present the key challenges that the FeFET technology currently faces w.r.t scaling, design-time and runt-time variability, read/write disturbance, and high write voltage. Then, I will present unprecedented dual-port FeFET which is completely disturb free demonstrating its ability to offer scaling down the FE layer thickness down to merely 3nm while still reliably storing 8 states (i.e., 3-bit MLC-FeFET). Further, I will explain how abstracted reliability models can be developed from device physics to circuits towards realizing HW/SW codesign for robust in-memory computing that outstandingly synergizes with and brain-inspired Hyperdimensional computing.

Session No: 40 | Session Title: Technologies for RF/mmwave/THz radio

Audi: 7 | 02:30 PM-04:15 PM | **Session Chair:** Dr. Eric Desbonnets
Track: RF, Millimeter and THz Technologies, Circuits and Systems (RF-THz)
Date: 13-Dec-22

40-1: Highly-Integrated mm-Wave Systems for Radar Applications in CMOS and SiGe Technologies (Invited Talk)
Start Time: 02:30 PM (30 Mins)
Speaker/Author: Prof. Vadim Issakov, Braunschweig University of Technlogy, Germany
Presenter: Prof. Vadim Issakov

Abstract: This talk focusses on system and circuit design considerations for highly-integrated radar transceivers in CMOS and SiGe HBT technologies. The speaker will first provide motivation for realization of radar sensors at mm-wave frequencies by showing the possible applications. Then, frequency band allocations for radar at mm-wave frequencies are discussed. Next, speaker will discuss system level consideration in detail, such as level budget calculation, phase noise considerations, and design of the analog baseband.
Next, technology-dependent considerations and challenges related to critical building blocks are discussed. Then, the speaker will present several design examples of integrated radar transceivers operating at 60-GHz, 140-GHz and 300-GHz and will discuss the circuit architectures. The talk is rounded out by a vision and trends in MIMO radar array realizations.

40-2: Challenges of on-wafer S-parameter characterization of advanced SiGe HBTs at very high frequencies (Invited Talk)
Start Time: 03:00 PM (30 Mins)
Speaker/Author: Prof. Thomas Zimmer, University of Bordeaux, France
Presenter: Prof. Thomas Zimmer

Abstract: In this talk, we will provide an overview of the challenges that can arise when measuring S-parameters at high frequencies, such as:
- The design of test structures for on-wafer TRL calibration
- The assessment of off-wafer versus on-wafer calibration methods
- The analysis of the impact of the probe geometry on the measurement results
- The investigation of the coupling with neighboring structures
Solutions to improve the measurement quality are also proposed. The presentation concludes with a comparison of the transistor measurements with the HBT compact model "HiCuM", focusing on the distributed and non-quasistatic effects.

40-3: Terahertz Field Driven Active Switching in Vanadium Dioxide-Based Multilayer Metasurfaces (Oral)
Start Time: 03:30 PM (15 Mins)
Speaker/Author: Soumyajyoti Mallick and Dibakar Roy Chowdhury (Mahindra University, India)
Presenter: Soumyajyoti Mallick

Abstract: We propose a multilayer meta-device in metal/insulator/metal configuration that exploits broadside coupling of the incident THz radiation to the meta-structure mediated through the VO2 spacer layer. We theoretically demonstrate that, by changing the field strength of the incident radiation, the field confinement and thus, the spectral response of the structure can be modulated by means of initiating insulator to metal phase transition in VO2 spacer layer by exploiting the strong electron-electron correlation in such structures. Hence, the all-optical modulation of the THz field can be attained by means of active tuning. The outcomes of our work hold tremendous potential in attaining active control of metamaterials by all-optical route as well as pave the way for ultrafast sensing, switching applications and nonlinear studies.

40-4: Terahertz Silicon Topological Photonics for 6G communications (Invited Talk)
Start Time: 03:45 PM (30 Mins)
Speaker/Author: Prof. Ranjan Singh, NTU Singapore
Presenter: Prof. Ranjan Singh

Abstract: Global digitalization and the recent rise of artificial intelligence-based data-driven applications have directed their vectors towards terabits per second (Tbps) communication links. The fast-evolving 5G communication network cannot fulfill this demand due to several technological challenges, including bandwidth scarcity, which has stimulated innovative technologies with a vision of 6G communication. Terahertz (THz) technologies have been identified as a critical candidate for the emerging 6G communication with the potential to provide ubiquitous connectivity and remove the barrier between the physical, digital, and biological worlds. Nonetheless, the existing THz photonic on-chip communication devices suffer from backscattering, bending loss, limited data speed, and lack of active tunability. Here, I will describe a new class of on-chip THz photonic topological devices consisting of low-loss, broadband single channel 160 Gbit/s communication link and critically coupled high-Q (Q ~ 106) cavities built on Silicon Valley-Hall Photonic Crystal. Silicon topological photonics will pave the path for augmentation of CMOS-compatible hybrid electronic-photonic driven terahertz technologies, vital for accelerating the development of 6G communications that would empower societies with real-time terabits per second wireless connectivity for network sensing, holographic communication, cognitive internet of everything, and massive digital cloning of the physical and the biological world.

Session No: 41 | Session Title: Other Emerging Devices & Compute Technology - 2

Audi: 8 | 02:30 PM-04:15 PM | **Session Chair:** Prof. Nihar Mohapatra
Track: Other Emerging Devices & Compute Technology (EDCT)
Date: 13-Dec-22

41-1: Voltage control of nanoscale magnets: energy efficient non-volatile memory, neuromorphic computing and quantum control of spin qubits (Invited Talk)
Start Time: 02:30 PM (30 Mins)
Speaker/Author: Prof. Jayasimha Atulasimha, Virginia Commonwealth University
Presenter: Prof. Jayasimha Atulasimha

Abstract: The key problem with magnetic random access memory (MRAM) is the high current requirement and energy dissipation to write information. This can be solved with electrical field control of magnetization in nanoscale magnets that have the potential to be extremely energy efficient. Our group's research focuses on using this paradigm towards implementation of energy efficient non-volatile memory [2], neuromorphic computing devices [3] such a quantized synapses and reservoir computers amenable to implement on edge/IoT devices. Furthermore, by tuning the frequency of the such nanomagnet's electric field drive to the Larmor frequency of spin qubits, single-qubit quantum gates with fidelities needed for fault-tolerant quantum computing [4] can be implemented. These device applications will be discussed.

References: [1] Nature Electronics 3, 539, 2020; [2] https://arxiv.org/abs/2112.13527 [3] https://arxiv.org/abs/2203.16720

41-2: An insect-inspired collision detector based on atomically thin and light-sensitive 2D memtransistors (Invited Talk)
Start Time: 03:00 PM (30 Mins)
Speaker/Author: Prof. Saptarshi Das, Penn State University, USA
Presenter: Prof. Saptarshi Das

Abstract: Collision detection under poor illumination and nightly conditions pose significant challenge for manned and unmanned vehicles, flying drones, and robots navigating complex terrestrial and extraterrestrial geographies. Existing night vision cameras offer solution based on sophisticated enhancement algorithms or additional thermal sensors necessitating extensive and expensive hardware, which make them power-hungry and untenable for deployment in remote and resource constrained locations. In contrast, nocturnal flying insects can avoid collision using very limited neural resources. Insect-inspired collision detectors based on silicon complementary metal oxide semiconductor technology and field programmable gate arrays also exist, however, the physical separation between sensing and compute and absence of spike-based information processing capability increases their area and energy overhead. Here, we introduce an insect-inspired, spike-based, and in-sensor collision detector using a reconfigurable optoelectronic integrated circuit constructed based on atomically-thin and light-sensitive memtransistors. We imitate the escape response of lobula giant movement detector (LGMD) neuron found in many insect species and demonstrate timely collision detection for various real-life scenarios at night involving cars on collision course. Our collision detector has a small effective footprint of 40 μm2 and consumes miniscule energy of few hundreds pico-Joules.

41-3: Micromagnetic Simulations of Magnetization Dynamics Due to Position-Dependent Spin-Orbit Torque From Topological Insulator (Oral)
Start Time: 03:30 PM (15 Mins)
Speaker/Author: Vinod Naik Bhukya and Rik Dey (IIT Kanpur, India); Yogesh Chauhan (Indian Institute Of Technology, India)
Presenter: Vinod Naik Bhukya

Abstract: A micromagnetic simulation study has been performed to analyze the magnetization switching dynamics of a ferromagnet on a topological insulator surface. The micromagnetic simulation is based on an analytical solution obtained for the spin-orbit torque which is position-dependent due to current shunting in the bilayer. The micromagnetic simulation is carried out using Ubermag, which is a python-language-based interface and uses OOMMF as the computational backend. From the simulations, switching times are extracted for the position-dependent case as well as various limiting cases. It is found that the switching time for the position-dependent case approaches the parallel transport limit for large values of the normalized tunneling rate and large length of the device, and the spin-orbit torque efficiency can be greater than 1 in those cases.

41-4: The role of heterogeneous integration in emerging device development (Invited Talk)
Start Time: 03:45 PM (30 Mins)
Speaker/Author: Prof. Subramanian Iyer, University of California, Los Angeles
Presenter: Prof. Subramanian Iyer

Abstract: Title: The role of heterogeneous integration in emerging device development
Session TBD

Abstract: While heterogeneous integration has always been practiced in electronics packaging, the scale in conventional packaging has been macroscopic with packaged dies or chips integrated on a printed circuit board at ball grid array pitches of several hundred micrometers and trace pitches of tens of micrometers and inter die

distances in the range of a few to several mm. In the last several years, the advent of more silicon-like substrates and the adoption of silicon technology, these dimensions have scaled considerably. At UCLA chips for example we have pioneered sub-10□m bump pitches, inter-die spacings of tens of □m, and wafer scale integration. Other approaches such as pseudo-monolithic integration where disparate devices and materials are assembled on say on processed silicon and interconnected lithographically at a ~100 nm scale pitches promise to upend the potential of classical approaches of trying to integrate everything on a CMOS wafer. In this talk, we will review these developments, their potential and also address some of the limitations. These new developments are indeed commercially viable and will lead to increased functionality at lower cost and size, enabling a "Moore's Law" at the system level.

Session No: 42 | Session Title: ESD Devices & SoC Design
Audi: 9 | 02:30 PM-04:15 PM | **Session Chair:** Dr. N. S. Kranthi (TI)
Track: Electrostatic Discharge Reliability (ESD) & ULSI Circuits/System-on-Chip/Power SoC (SoC)
Date: 13-Dec-22

42-1: On-chip ESD protection design with consideration for system level ESD and immunity test of EMC (Invited Talk)
Start Time: 02:30 PM (30 Mins)
Speaker/Author: Mr. Mototsugu Okushima, Renesas Electronics, Japan
Presenter: Mr. Mototsugu Okushima

Abstract: Characteristics of on-chip ESD protection circuitry is becoming larger factor to determine results of the system level ESD test or immunity test of EMC after mounting IC on the board. In these test cases, characteristics of on-chip ESD circuitry can show different behavior from that of unpowered condition of inherent component level ESD test. On-chip ESD design examples with consideration for powered condition like system level ESD test and much longer pulse condition like an immunity test unlike nano second pulse like ESD test will be presented. These design techniques can make harmonized design with off-chip ESD device more flexible. On-chip ESD sensor to observe current injected into IC at system level ESD will also presented.

42-2: On the ESD Behavior of Hydrogenated Amorphous Silicon Based High- Voltage TFTs (Oral)
Start Time: 03:00 PM (15 Mins)
Speaker/Author: Rajat Sinha (Indian Institute of Science, India); Sanjiv Sambandan (Indian Institute of Science, Bangalore, India & University of Cambridge, United Kingdom (Great Britain)); Mayank Shrivastava (Indian Institute of Science Bangalore, India)
Presenter: Rajat Sinha

Abstract: In this paper, we present detailed physical insights into the electrostatic discharge (ESD) behavior of high-voltage amorphous silicon (a-Si: H) thin-film transistors (TFTs). Device architecture which provides a 4-5x times improvement in ESD robustness with the same spatial considerations is discussed. The physics behind the improvement in ESD robustness is explored, and technological parameters' impact on ESD behavior is studied. Transmission line pulse (TLP) characteristics are discussed, and the failure behavior is explored.

42-3: On the ESD Behavior of a- Si: H Based Diode-Connected Thin- Film Transistors (Oral)
Start Time: 03:15 PM (15 Mins)
Speaker/Author: Rajat Sinha (Indian Institute of Science, India); Sanjiv Sambandan (Indian Institute of Science, Bangalore, India & University of Cambridge, United Kingdom (Great Britain)); Mayank Shrivastava (Indian Institute of Science Bangalore, India)
Presenter: Rajat Sinha

Abstract: This work presents physical insights into the operation and ESD behavior of a-Si: H based diode-connected thin-film transistors. The device operation is studied through DC I-V characterization and the device leakage under normal conditions are explored. The ESD behavior is then explored and a three-stage device behavior is observed. It is observed that the device fails due to electric field lead thermal breakdown. The impact of pulse width and channel dimensions are studied. Finally, the device behavior under negative ESD stress is studied and it is found that application of negative ESD stress presents a delayed turn- on behavior owing to depletion of charge carriers under negative gate bias.

42-4: ESD Behavior of Fin Based Tunnel FETs (Oral)
Start Time: 03:30 PM (15 Mins)
Speaker/Author: Harsha B Variar (Indian Institute of Science, India); Kranthi Nagothu (Texas Instruments, India); Hemanjaneyulu Kuruva and Mayank Shrivastava (Indian Institute of Science Bangalore, India)
Presenter: Harsha B Variar

Abstract: This paper investigates the reliability of a novel Fin-enabled vertical or area-scaled tunnelling FET proposed for sub-10-nm channel length operation. This device enables a smooth transition from FinFET technology to Fin-based vertical TFETs, while enjoying the benefits of FinFET architecture. To make this device commercial, it's important to understand the reliability performance of this device. This work explores the reliability physics of this device with detailed physical insight into the device operation and failure under ESD stress conditions. The proposed device has a deep N+ implant underneath the P+ source for the ESD protection applications, which has resulted in twice improvement in ESD failure current with less area overhead. The proposed concept can also be extended to the different class of tunnelFETs like Vertical/Area Scaled TFETs. The impact of various technology(SOI and Bulk) and device design parameters on the ESD behavior and robustness of Fin-based TFETs is discussed. This has helped developing guidelines to design ESD robust or efficient protection concepts.

42-5: GBRHQ-14T: Gate-Boosted Radiation Hardened Quadruple SRAM Design (Oral)
Start Time: 03:45 PM (15 Mins)
Speaker/Author: Pramod Kumar Bharti and Joycee Mekie (IIT Gandhinagar, India)
Presenter: Pramod Kumar Bharti

Abstract: Radiations in space are very critical and may cause failure in the SRAM. Various state-of-the-art SRAMs, such as DICE, Quatro-10T, etc., are proposed to mitigate the failure of SRAM. However, the designs are still vulnerable to radiations causing soft errors. This work proposes a Gate Boosted Radiation Hardened Quadruple 14T SRAM with better Single Node Upset (SNU) and Double Node Upset (DNU) tolerance. It has very high read stability. On top of that, our proposed design outperforms in terms of RSNM, Read Access Time(RAT), Wordline Write Trip Voltage (WWTV), Write Access Time (WAT), and leakage power than most conventional designs. It has a maximum of 1.3x less RAT than SAR-14T, 2.63x more WWTV than Quatro-10T, 1.38x less WAT than Quatro-10T SRAM, and 1.32x less leakage power than SEA-14T SRAM respectively at VDD=0.9V, CMOS 28nm Technology.

42-6: Machine Learning Based Flip-Flop Clustering for Clock Network Power Improvement (Oral)
Start Time: 04:00 PM (15 Mins)
Speaker/Author: Santanu Kundu (Intel Technology India Pvt. Ltd. & Bangalore, India); Niraj A Mehta and Arpan Sircar (Intel Technology India Pvt. Ltd., India)
Presenter: Santanu Kundu

Abstract: Power reduction is one of the key challenges in today's SoC implementation. In this work, we have presented an unsupervised Machine Learning based multi-bit flip-flop clustering and relocation framework to address the clock network power reduction without impacting the performance of the design. During clustering of multi-bit flip-flops, localized congestion is experienced. This paper has shown how to mitigate the congestion issue by controlling the cluster size and flop displacement limit. Implementation on external foundry process node shows that our proposed methodology can reduce significant clock wirelength and clock network power, which is leading to 10%, 3%, and 2% reduction in total power respectively in three real industry designs.

Session No: 43 | Session Title: Power Electronics Systems and Applications

Audi: 10 | 02:30 PM-04:15 PM | **Session Chair:** Prof. Shankar Madathil
Track: Advanced Power Device Technology (APDT)
Date: 13-Dec-22

43-1: TVS Technology, Products and Applications (Invited Talk)
Start Time: 02:30 PM (30 Mins)
Speaker/Author: Dr. Shekar Mallikarjunaswamy, Alpha and Omega Semiconductor Ltd
Presenter: Dr. Shekar Mallikarjunaswamy

Abstract: Transient Voltage Suppressors (TVS) are primarily used on-board to protect sensitive I/O and power supply pins of Integrated Circuits (ICs) from being damaged by system level ESD (IEC61000-4-2 and IEC61000-4-5). Rapid growth in high-speed ports for USB and HDMI applications have increased the market demand for low capacitance protection products. Although, the system level ESD protection devices can be monolithically

integrated on-chip, the die cost increases. In addition, it is difficult to exceed the performance of standalone TVS that utilize special cost-effective process technology that is not available in advanced CMOS nodes. This talk will present the state-of-the-art TVS technology, package and product characterization for USB, HDMI and Ethernet applications.

43-2: Performance and Reliability Co-Design of Ultra High Voltage LDMOS Devices (Oral)
Start Time: 03:00 PM (15 Mins)
Speaker/Author: Harsha B Variar (Indian Institute of Science, India); Jhnanesh Somayaji (Srinivasnagar, India); Mayank Shrivastava (Indian Institute of Science Bangalore, India)
Presenter: Harsha B Variar

Abstract: This work presents the performance and reliability (HCI, SOA and ESD) co-design insights of Ultra High Voltage (UHV) Laterally Diffused Metal Oxide Semiconductor (LDMOS) devices. Device design insights and performance optimization guidelines for four different types of UHV LDMOS devices (Conventional, RESURF, SOI and RESURF SOI) is systematically developed using 3D TCAD. For the first time, a step-by-step approach to design gate, drain and source field plates and its implications on the co-design of these four different UHV designs is investigated, which demonstrated significant improvement in the device breakdown without altering its ON-resistance. Finally, performance and HCI, ESD & SOA reliability benchmarking is done for the optimum designs of all four (i.e. Conventional, RESURF, SOI and RESURF SOI) UHV LDMOS architectures.

43-3: Flip chip bonding of integrated circuits (Invited Talk)
Start Time: 03:15 PM (30 Mins)
Speaker/Author: Dr. Raghvendra Sahai Saxena, Solid State Physics Laboratory (DRDO), Delhi, India
Presenter: Dr. Raghvendra Sahai Saxena

Abstract: Flip chip bonding is used to connect semiconductor devices, integrated circuits, micro-electro-mechanical systems (MEMS) etc. with external circuitry or another integrated circuit using metal bumps deposited on the chip pads. This technology is quite common in high density interconnections in mega pixel focal plane array sensors. It can be utilized for getting millions of connections among the cells of a power MOSFET using micro bump array. A method of estimating the interconnection yield and connection reliability using daisy chain and fanout pattern on transparent substrates has been implemented. The results have been used for analysis and optimization of flip chip process.

43-4: Power Electronics Energy System (PEES) (Invited Talk - Withdrawn)
Start Time: 03:45 PM (30 Mins)
Speaker/Author: Prof. Alex Qin Huang, University of Texas at Austin
Presenter: Prof. Alex Qin Huang

Abstract: Driven by innovations in power semiconductor technology, decreased cost in solar, wind and energy storage technology, and the strong need to decarbonize every sector of our society, power electronics-based generations are positioned to replace today's synchronous generator as the governing generation technology in the future. Simultaneously, electrifications on the load side are also power electronics based, hence creating a power electronics energy system (PEES) that encompasses generation, transmission, distribution and load. Due to the flexible and fast controllability of power converters, PEES can potentially outperform today's energy system and achieve higher energy efficiency. A complete DC based PEES is also feasible. However, there are many challenges in designing and operating a PEES. This talk will provide an overview of power electronics technology, focusing on the state of the art from hardware and control point of view. New opportunities enabled by emerging power electronics technology in grid applications will be highlighted. The talk will also discuss gaps and research needs for a power-electronics based grid.

Session No: 44 | Session Title: Accelerators for Edge Intelligence

Audi: 11 | 02:30 PM-04:15 PM | **Session Chair:** Prof. Shubham Sahay
Track: Neuromorphic Device Technology, Circuits and Systems (NDTCS)
Date: 13-Dec-22

44-1: Low-power Edge Intelligence from an Industry Perspective (Invited Talk)
Start Time: 02:30 PM (30 Mins)
Speaker/Author: Dr. Arijit Mukherjee, Embedded Devices & Intelligent Systems, TCS Research, India
Presenter: Dr. Arijit Mukherjee

Abstract: The world is becoming increasingly connected, from autonomous vehicles, smart homes, personal robotics to space exploration. These AI-powered applications rely on fast, autonomous, near real-time analysis of diverse data from multiple sources. They are pushing the boundaries of computing - taking it closer to the edge, the point where data is collected, and analysed. Neuromorphic computing is expected to play an important role in advancing edge computing capabilities by mimicking the human brain and its cognitive functions such as interpretation and autonomous adaptation. It is a high-performance, ultra-low power alternative to the von Neumann architecture which is based on traditional bus-connected CPU-memory-peripherals. Due to the time and energy required to send information back and forth between the memory and the CPU, von Neumann machines do not have the ability to support the increasing computational power required by AI applications. At the same time, physical limitations in the size of transistor-based processor circuits impact energy efficiency. Evolving neuromorphic processors, which are designed to replicate the human brain, eliminate the von Neumann bottleneck. Inspired by the brain's adaptability and ability to support parallel computation, neuromorphic devices integrate processing and memory at higher speed, complexity, and better energy efficiency. This is critical for enabling intelligence at the edge and processing sparse events.

44-2: Performance improvement of machine learning hardware accelerators on FPGA (Invited Talk)
Start Time: 03:00 PM (30 Mins)
Speaker/Author: Prof. Nanditha Rao, International Institute of Information Technology, Bangalore, India
Presenter: Prof. Nanditha Rao

Abstract: CNN accelerators implemented using FPGAs can enable significant performance improvement. To fully utilize the computing capability of an FPGA, there is also a need to efficiently map the design on to the FPGA fabric. We observe that mapping the convolution operation onto pipelined DSP-adder tree (PDAT) structures results in a 2.4x improvement in frequency compared with a default baseline mapping. There is also growing interest in designing flexible FPGA fabrics with alternate physical locations of DSPs and Block RAMs. An initial step is to study the impact of the location of heterogeneous blocks on the performance of the ML benchmarks. We propose a new architecture which consists of clusters of heterogeneous blocks scattered across the FPGA layout. We observe that it results in 6.4% improvement in the critical path delay.

44-3: Performance of Graphene Oxide-Based Memristor for Nonvolatile Memory and Neuromorphic Computing (Oral)
Start Time: 03:30 PM (15 Mins)
Speaker/Author: Kanupriya Varshney (IIT Ropar & IIT, India); Mani Shankar Yadav (IIT Ropar, India); Devarshi Mrinal Das (Indian Institute of Technology Ropar, India); Brajesh Rawat (IIT Ropar, India)
Presenter: Kanupriya Varshney

Abstract: In this work, we investigate the performance of two-dimensional graphene oxide (GO)-based memristor and explore their advantages over the most popular metal oxide (TaO x)-based memristor for non-volatile memory and neuromorphic computing applications. The performance analysis of memristors is done using a self-developed numerical modeling framework,-based on self-consistent solutions of the continuity, Joule's heating, and current continuity equations. GO-based memristor has demonstrated excellent switching performance with significantly lower sneak current (5.41 μA), higher ON/OFF resistance (R on/R off = 200), higher read window (11.6), and higher non-linearity (106.4) than that for TaO x-based memristor. Further, a higher ON/OFF resistance ratio in a GO-based memristor promises a larger crossbar array size (2 6) over TaO x-based memristor counterpart with a minimum readout margin. Over GO-based memristor, the TaO x-based memristor exhibits linear and symmetrical conductance modulation with an identical applied pulse train, which makes them a more promising candidate for neuromorphic computing with probability of higher reading accuracy.

44-4: On-Chip Learning on Spintronic-Synapse-Based Crossbar Arrays: Device-Level Experiments and System-Level Simulations (Invited Talk)
Start Time: 03:45 PM (30 Mins)
Speaker/Author: Prof. Debanjan Bhowmik, Indian Institute of Technology Bombay, India
Presenter: Prof. Debanjan Bhowmik

Abstract: Non-volatile memory (NVM) devices that exhibit multiple electrically readable and controllable non-volatile conductance states have been widely considered as synaptic elements in analog crossbar arrays for fast and low-energy implementation of neural network (NN) algorithms. In this talk, I first show through experiments and micromagnetic simulations that in a heavy-metal ferromagnetic-metal-heterostructure-based spintronic device exhibiting perpendicular magnetic anisotropy, multiple such electrically controllable non-volatile states corresponding to different magnetization configurations are possible, making the device suitable for a synapse.

Next, I show device-circuit-system co-design and co-simulation of crossbar arrays using these spintronic synapses and demonstrate on-chip learning of fully connected neural networks (FCNNs) and convolutional neural networks (CNNs) through them for image classification.

Session No: 45 | Session Title: Graphene and related materials
Audi: 1 | 04:30 PM-05:45 PM | **Session Chair:** Prof. Luis A Jauregui
Track: 2D Material Based Technologies (2DT)
Date: 13-Dec-22

45-1: Understanding Interface Conductivity of Graphene with Oxide Semiconductors (Invited Talk)
Start Time: 04:30 PM (30 Mins)
Speaker/Author: Dr. Krishna B Balasubramanian, Indian Institute of Technology Delhi, India
Presenter: Dr. Krishna B Balasubramanian

Abstract: Oxide semiconductors are technologically promising for several opto-electronic applications. However, Interface conductivity with the semiconductor has been a major issue due to low electron affinity values of the semiconductor and the identification of a good Ohmic contact will be in the interest of device engineers from diverse fields. Using Cu2O we experimentally measure contact resistance with different metals systematically as well as with graphene, a transparent conducting monolayer. Using first principles calculations we justify the measurements as well as observe that graphene-Cu2O heterojunction work function strongly varies with the atomic configuration of the surface. The oxygen terminated surface of Cu2O is observed to have an Ohmic interface for holes making graphene a good transparent interface for Cu2O based hole transport layers of photovoltaics and photon detectors.

45-2: Tilted Graphene Junctions for Valleytronics Applications (Oral)
Start Time: 05:00 PM (15 Mins)
Speaker/Author: Shrushti Tapar and Bhaskaran Muralidharan (Indian Institute of Technology Bombay, India)
Presenter: Shrushti Tapar

Abstract: Valleytronics is one of the disruptive technologies, being explored for quantum computing. Valley qubits are more robust to external environmental perturbations compared to conventional charge-based qubits. In order to develop valleytronic devices, achieving valley polarization is paramount. Various 2D materials have been widely explored for realizing valley-based devices because of their unique band structure. Most of these proposed works used the scattering mechanism with line defects, strain barriers, and magnetic barriers. However, they are limited by low transmission values and changes in polarization directionality. In order to overcome these issues, we propose an electrostatically tuned valley polarizer device that incorporates a simple tilted graphene PN junction. The tilted interface scatters Fermions anisotropically based on the valley index. The device variables like tilt angle, junction transition width, position, and electron energy determine polarization. We performed numerical simulations using the scattering matrix approach for analyzing the underlying physics and summarized the optimal conditions for achieving maximum polarization.
45-3: 2D Dielectric Materials for Emerging Nanoelectronic Devices (Invited Talk)
Start Time: 05:15 PM (30 Mins)
Speaker/Author: Dr. Shubhakar Kalya, Singapore University of Technology and Design (SUTD), Singapore
Presenter: Dr. Shubhakar Kalya

Abstract: Two dimensional (2D) dielectric materials are amongst the key drivers enabling the realization of next generation nanoelectronic devices in the future [1]. Hexagonal boron nitride (h-BN), 2D mica and Fluorinated graphene have recently attracted a lot of attention as 2D dielectric materials [2,3]. In particular, h-BN emerges as one of the promising dielectric materials for graphene and other 2D layered semiconductor based nanoelectronic devices. The h-BN exhibits perfect match for graphene as they share many similarities. Mica dielectric material used as a substrate for various heterogeneous 2D material structures due to its excellent thermal stability, surface flatness, light transmittance and chemical resistance. Fluorinated graphene is another 2D dielectric material which demonstrates excellent dielectric properties with fast and scalable processing. Importantly, there is limited insight and conclusive evidence on the physics of degradation, reliability and breakdown (BD) in these 2D dielectric materials. Here, we highlight important findings on the mechanism of degradation and BD in h-BN and Mica dielectrics from the device level to localized nanometer scale regions of 2D dielectrics. Nanoscale analysis tools (Conductive atomic force microscopy (CAFM) and transmission electron microscopy (TEM)) are used to assess the nanoscale performance of the 2D dielectrics; local degradation due to dielectric wear-out and subsequent breakdown.

Session No: 46 | Session Title: New approaches and Advanced Devices
Audi: 2 | 04:30 PM-06:00 PM | **Session Chair:** Prof. K. L. Narasimhan
Track: Solar Cells & Photodetectors: Physics, Device, & Modules (SP)
Date: 13-Dec-22

46-1: Pushing limits of photovoltaics and photodetection using radial junction nanowire devices (Invited Paper)
Start Time: 04:30 PM (30 Mins)
Speaker/Author: Vidur Raj (University of Glasgow, United Kingdom (Great Britain)); Yi Zhu (University of Cambridge, United Kingdom (Great Britain)); Kaushal Vora (The Australian National University, Australia); Lan Fu (Australia National University, Australia); Hoe Tan and Chennupati Jagadish (Australian National University, Australia)
Presenter: Vidur Raj

Abstract: Nanowire devices have long been proposed as an efficient alternative to their planar counterparts for different optoelectronic applications. Unfortunately, challenges related to the growth and characterization of doping and p-n junction formation in nanowire devices (along axial or radial axis) have significantly impeded their development. The problems are further amplified if a p-n junction has to be implemented radially. Therefore, even though radial junction devices are expected to be on par with their axial junction counterparts, there are minimal reports on high-performance radial junction nanowire optoelectronic devices. This paper summarizes our recent results on the simulation and fabrication of radial junction nanowire solar cells and photodetectors, which have shown unprecedented performance and clearly demonstrate the importance of radial junction for optoelectronic applications. Our simulation results show that the proposed radial junction device is both optically and electrically optimal for solar cell and
photodetector applications, especially if the absorber quality is extremely low. The radial junction nanowire solar cells could achieve a 17.2% efficiency, whereas the unbiased radial junction photodetector could show sensitivity down to a single photon level using an absorber with a lifetime of less than 50 ps. In comparison, the axial junction planar device made using same substrate as absorber showed less than 1% solar cell efficiency and almost no photodetection at 0 V. This study is conclusive experimental proof of the superiority of radial junction nanowire devices over their thin film or axial junction counterparts, especially when absorber lifetime is extremely low. The proposed device holds huge promise for III-V based photovoltaics and photodetectors.

46-2: Low-Field Electron Transport Study of III-V Type-II Superlattices (Oral)
Start Time: 05:00 PM (15 Mins)
Speaker/Author: Rohit Kumar and Anup Kumar Mandia (Indian Institute of Technology Bombay, India); Anuja Singh and Bhaskaran Muralidharan (IIT Bombay, India)
Presenter: Rohit Kumar

Abstract: Type-II superlattice (T2SL) has the ability to operate at high temperatures and overcome the drawbacks of mercury cadmium telluride (MCT or HgCdTe), which has been the
most widely used detector, in terms of size, range, resolution, weight, and power consumption. Third-generation detectors with a wide range of applications are frequently designed using T2SLs based on InAs/GaSb. An extensive analysis of the semi-classical transport model derived from the Boltzmann transport equation (BTE) is presented in this research. To describe the electron transport properties of 8ML/8ML InAs/GaSb T2SL, we employ Rode's algorithm, which explicitly addresses relevant physical aspects such as elastic and inelastic scattering mechanisms. We calculate the electron drift mobility and conductivity in conjunction with the k.p band structure model. Ionized impurity (II), piezoelectric (PZ), polar optical phonon (POP), acoustic deformation potential (ADP), and interface roughness scattering (IRS) are five scattering processes that are included in our study. In relation to temperature, structural parameters, and the concentration of carriers, the estimated mobilities and conductivities display a variety of behavior.

46-3: Photo-Response and Memory Effect Resemblance of Piezoceramics Adapted in Photovoltaic Architecture (Oral)
Start Time: 05:15 PM (15 Mins)
Speaker/Author: Apoorva Singh, Digvijay Narayan Singh and Ram Prakash Singh (Indian Institute of Science Bengaluru, India); Rajeev Ranjan and Praveen C Ramamurthy (Indian Institute of Science, India)
Presenter: Apoorva Singh

Abstract: Here the light responsivity of electrically poled ferroelectric piezoceramics with the composition (0.3) BiFeO3- (0.7) Pb0.95La0.05 (Zr0.57Ti0.43)0.9875O3 (BFPTZT) through electrical current-voltage (IV) characterizations in dark and 1 Sun (AM 1.5 G) illumination were evaluated. Distinct current features (~ 10 nA)

are observed from a thin solid pallet in the presence of light than dark, indicating light sensitivity. The material in the finely grained powdered form is introduced in the PEDOT: PSS, a hole transport layer of perovskite solar cell. Both poled, and unpoled samples resulted in different characteristics than the reference devices. The poled-BFPTZT-based device is found to be substantially perturbed with the light exposure and duration with the characteristics resembling memory effect, potentially arising due to the photoactivated domain alignments.

46-4: Molecular Engineering of π-Functional Conjugated Materials for Photonics, Electronics, and Sensing (Invited Talk)
Start Time: 05:30 PM (30 Mins)
Speaker/Author: Prof. Prashant Murlidhar Sonar, Queensland University of Technology
Presenter: Prof. Prashant Murlidhar Sonar

Abstract: Next generation active electronic materials used in devices are undergoing continual improvements to generate devices that are high performance, lighter, flexible, stretchable, and more energy efficient with lower cost. Carbon based novel solution processable π-functional conjugated materials are the focus of intense academic and industrial research since they are important class of soft materials for large area electronics including transistors, displays, sensors and light harvesting devices. The active organic semiconducting materials are emerging due to their tunable light absorption/emission, interesting charge transport properties, relatively adequate HOMO-LUMO energies and ink formulation capability. In my talk, I will explain the various classes of conjugated carbon-based materials either as polymers, small molecules or quantum dots prepared via chemically and electrochemically using various novel aromatic conjugated building blocks. In this presentation, the design, synthesis, optoelectronic properties, and device performance of novel advanced materials for field effect/electrochemical transistors, perovskite solar cells, light emitting diodes, optical sensors and various sensing devices will be discussed. Such materials and devices have great potential in future electronics, energy, health, and environmental monitoring.

Session No: 47 | Session Title: GaN and SiC Device Technology & Physics - 1
Audi: 3 | 04:15 PM-06:00 PM | **Session Chair:** Dr. Kamal Varadarajan
Track: Wide Bandgap Power Semiconductor Technologies (WPSD)
Date: 13-Dec-22

47-1: A Comparative study of GAN-on-silicon with SiC Devices in the 5KW-10KW Power range (Invited Talk)
Start Time: 04:15 PM (30 Mins)
Speaker/Author: Mr. Prasad Joshi, Transphorm, USA
Presenter: Mr. Prasad Joshi
Abstract: GaN-on-Silicon transistors are gaining traction in the field of AC/DC and DC/DC high voltage power electronics for power levels ranging from 45W to over 10kW. Especially in the power levels ranging from 500W to 10kW, bridge topologies such as totem-pole PFC, half-bridge or full bridge converters, inverters etc. are very popular. In this power range, there is always a tussle between GaN-on-Silicon and Silicon Carbide power devices in terms of efficiency and switching frequencies. In the 650V or 900V class of power devices for these power ranges and topologies, it is important to establish the leader in terms of power density, solution temperature and as well as ease of implementation. This paper and presentation provides a direct comparison of leading GaN-on-Silicon devices and its equivalent Rds(on) Silicon Carbide devices in terms of switching characteristics, reverse conduction, reverse recovery, gate driving that can explain the differences in efficiency at various switching frequencies. The quantum effects will not be considered as this paper will focus on experimental results. In the paper, industry's leading Transphorm GaN-on-Silicon devices will be compared with leading Silicon Carbide MOSFETs.
47-2: Dynamic performance of wide bandgap devices (Invited Talk)
Start Time: 04:45 PM (30 Mins)
Speaker/Author: Dr. Carlo De Santi, University of Padova, Italy
Presenter: Dr. Carlo De Santi

Abstract: This presentation will review some important non-idealities causing a lower dynamic performance in wide bandgap power devices. After an introduction on the most relevant wide bandgap semiconductors, the experimental analysis and modeling of the surface effects will be presented, based on a physically-consistent theoretical modeling of the stretched exponential function. A complete model for the conduction processes in isolation structures will be developed, based not only on the emission behavior but also on the filling kinetics. Finally, the trapping mechanisms in gate insulators causing a logarithmic time dependence of the filling and recovery processes will be investigated according to the inhibition model.

47-3: Unique Role of Carrier Transport Through Carbon Doped GaN Buffer in Determining Breakdown Behavior of Normally-OFF Cascode AlGaN/GaN HEMTs (Oral)
Start Time: 05:15 PM (15 Mins)
Speaker/Author: Vipin Joshi, Sayak Dutta Gupta and Rajarshi Roy Chaudhuri (Indian Institute of Science, India); Mayank Shrivastava (Indian Institute of Science Bangalore, India)
Presenter: Vipin Joshi

Abstract: We report a unique reduction in the breakdown voltage of a normally -ON AlGaN/GaN HEMT when used in a cascode configuration with a normally-OFF LDMOS device. This reduction in breakdown voltage is found to be due to the early breakdown of the LDMOS. Detailed analysis reveals the breakdown voltage of the cascode HEMT to be a strong function of the carrier transport through the C-doped GaN buffer.

47-4: Latest Progress on GaN Power Device Technologies for EV Applications (Invited Talk)
Start Time: 05:30 PM (30 Mins)
Speaker/Author: Dr. Davide Bisi, Transphorm Inc., U.S.A.
Presenter: Dr. Davide Bisi

Abstract: GaN power devices are penetrating and improving the efficiency of several consumer applications, including power adapters, power supplies, and DC/DC converters. The next step for GaN is to enter the electric vehicle, where it can boost the efficiency of on-board chargers, auxiliary DC/DC converters and powertrains. As GaN devices enter the EV, a new realm of challenges must be tackled and overcome. In this talk, we'll review present and future GaN technologies to succeed: high quality and reliability, large periphery 650-V GaN devices for high-power OBCs and powertrains; short-circuit capability for fail-safe operations; 1200-V rating for future 800-V batteries; and bi-directional switches for innovative, more efficient inverter topologies.

Session No: 48 | Session Title: Nanomaterials based Sensors

Audi: 4 | 04:30 PM-05:30 PM | **Session Chair:** Prof. Praveen Ramamurthy
Track: Sensors and Bio-electronics (SBE)
Date: 13-Dec-22

48-1: Fabrication of Ag2S, Bi2S3 and CdS p-FETs Using Solution Processing (Oral)
Start Time: 04:30 PM (15 Mins)
Speaker/Author: Gopal S. Pranjale, Suyog Ingle and Ganesh C. Patil (Visvesvaraya National Institute of Technology Nagpur, India)
Presenter: Gopal S. Pranjale

Abstract: Comprehensive study on chemically synthesized silver sulfide (Ag2S), bismuth sulfide (Bi2S3) and cadmium sulfide (CdS) field effect transistors (FETs) has been carried out. Physical characterization results and the in-depth electrical characterization show that the fabricated devices are functioning as the p-channel FETs. At channel length of 3 mm and the gate-to-source potential of -15 V, the ON-state current of the fabricated CdS, Bi2S3 and Ag2S p-FETs is found to be -8.5, -20.8 and -38.1 μA respectively. Furthermore, at drain-to-source potential of -10 V, the threshold voltage of -6.1, -5.2 and -6.08 V with OFF-state current of -0.07, -0.17 and -0.27 μA is measured for CdS, Bi2S3 and Ag2S p-FETs respectively. All the devices fabricated through simple, low-cost and industry scalable chemical route which opens a new era for fabricating the II-VI compounds (CdS), I-VI compounds (Ag2S) and V-VI compounds (Bi2S3) based FETs. The fabricated FETs seems to be more suited for the electrochemical sensors, optoelectronic circuits and the electronic circuit applications.

48-2: Performance Optimization and Analysis of a Work Function Engineered 20nm Grooved Channel Junctionless FinFET for Hydrogen Sensing (Oral)
Start Time: 04:45 PM (15 Mins)
Speaker/Author: Tejaswini Sahoo (National Institute of Technology, Rourkela, India); Prasanna Kumar Sahu (N. I. T. Rourkela, India); Annada Shankar Lenka (National Institute of Technology Rourkela, India)
Presenter: Tejaswini Sahoo

Abstract: A novel grooved channel, or raised source and drain junctionless FinFET (Fin Field effect transistor), has been developed in this study as a hydrogen gas (H2) sensor. The Visual TCAD simulator examines the response of junctionless FinFET for hydrogen gas detection. Platinum is employed as a catalytic metal gate. Variations in the concentration of gas molecules alter the pressure on the catalytic metal gate, influencing the metal work function. The presence of hydrogen is detected by the change in metal gate work function. The surface

potential, threshold voltage, drain current, and transconductance of the developed gas sensor extracted and analyzed. The device performance is tested for hydrogen gas concentration from 10-14 torr to 10-10 torr.

48-3: Sulphur-Doped Carbon Nanospheres Based Sensor for the Electrochemical Detection of Cadmium (Oral)
Start Time: 05:00 PM (15 Mins)
Speaker/Author: Radhika Varshney (Indian Institute of Science, Bangalore, India); Pavithra N (INDIAN INSTITUTE OF SCIENCE, India); Simranjeet Singh, T S Sunil Kumar Naik and Praveen C Ramamurthy (Indian Institute of Science, India)
Presenter: Radhika Varshney

Abstract: Cadmium (Cd), popularly used in electroplating, batteries, and paints, is a well-recognized carcinogen and a toxic non-essential element for the human body. Hence, developing an effective sensor for detecting Cd (II) from water is a critical requirement. In this work, an electrochemical sensor based on green synthesized sulphur-doped carbon nanospheres (S-CNs) modified carbon paste electrode (S-CNs/CPE) has been developed that demonstrates a limit of detection (LOD) of ~14.4 μM towards Cd (II) in water using differential pulse voltammetry (DPV) technique. Interference studies and real sample analysis reveal the effectiveness of the developed S-CNs/CPE.

48-4: Evidence for the Successful Manipulation of a Magnetic Nanorobot Inside the Hard Tumor of a Live Animal (Oral)
Start Time: 05:15 PM (15 Mins)
Speaker/Author: Sayanta Goswami, Debayan Dasgupta and Reshma Vasantha Ramachandran (Indian Institute of Science, India); Anaxee Barman (IISc, India); Ambarish Ghosh, Ramray Bhat and Deepak K. Saini (Indian Institute of Science, India)
Presenter: Sayanta Goswami

Abstract: Observation of nano/micron-scale objects inside living tissue is a significant challenge in all nanoparticle drug delivery research. Helical Magnetic Nanorobots[1] (HMNs) also face this problem, where any translation due to a rotating magnetic field is not readily observable. The problem arises due to the scattering nature of living tissue. Here we demonstrate a new technique to determine if HMNs have achieved translation by post-experimental analysis of tissue. We use non-magnetic tracer particles to identify the site of injection. The diffusive spread of HMNs is minimal due to the rigidity of the tissue. By observing the microtome slices of the tissue, we could observe HMNs far from their injection site, which would be possible only due to magnetic field-induced translation. This allows us to calculate the pitch of HMNs inside a living tissue to be about 20-25 nm.

Session No: 49 | Session Title: Displays: Design, Fabrication,and Processing

Audi: 5 | 04:30 PM-06:00 PM | **Session Chair:** Prof. Monica Katiyar
Track: Macroelectronics & Displays: Devices, Circuits & Systems (DIS)
Date: 13-Dec-22

49-1: Development of passive matrix displays based on thermo- and electro-chromic materials (Invited Talk)
Start Time: 04:30 PM (30 Mins)
Speaker/Author: Dr. Parasuraman Swaminathan, Indian Institute of Technology, Madras, India
Presenter: Dr. Parasuraman Swaminathan

Abstract: Flexible, lightweight, and low-power displays are an active area of interest in the electronics community. In this talk, I will focus on our group's work on developing displays based on thermochromic and electrochromic materials. Thermochromic materials are those that change colour due to a change in temperature. By combining with silver nanowires, we have synthesized printable inks that can change colour, mediated by Joule heating. An additional touch functionality can be enabled by encapsulating these materials and some prototypes will be highlighted. Electrochromic materials show a colour change by a change in oxidation state. Typically, transition metal oxides are used for these applications. I will highlight our group's work in developing nickel and tungsten oxide films, through low temperature processing routes, for electrochromic displays.

49-2: Design of a Low-Voltage and Reduced Programming Cycle AMOLED Pixel Circuit Using IGZO TFTs (Oral)
Start Time: 05:00 PM (15 Mins)
Speaker/Author: Divya Dubey (Indian Institute of Information Technology Allahabad, India); Manish Goswami (Indian Institute of Information Technology, India); Kavindra Kandpal (Indian Institute of Information Technology Allahabad, Prayagraj, India)
Presenter: Divya Dubey

Abstract: This work presents a 5T-2C pixel circuit based on amorphous indium gallium zinc oxide (a-IGZO) thin film transistors (TFTs) for flexible displays utilizing improved stacked voltage-programmed pixel circuit topology. Due to a low operating voltage of 5 V and reduced programming time of 8 μs, the proposed circuit finds its application in large screen HD displays as it can provide a very high frame rate of 120 Hz. Moreover, a good compensation ability of the proposed circuit against the threshold voltage variations of the driving TFT in the range of -0.2 volts to 2 volts from the nominal voltage of 0.7 volts, makes it suitable for flexible AMOLED displays. The error in organic light emitting diode (OLED) current is within 0.4% over the range of data voltage (3.8 V to 6 V) when the substrate is subjected to both compressive and tensile strains of ± 0.3 % and within 10% due to threshold voltage variations under electrical stress. The adapted SPICE level-3 flexible TFT model efficiently captures the variations in threshold voltage due to mechanical as well as electrical stress. As a result, the proposed 5T2C pixel circuit reveals good performance for applications in low-voltage flexible displays.

49-3: Solution-Processed Organic Light-Emitting Diodes With Slot-Die Coated Electron Transport Layer (Oral)
Start Time: 05:15 PM (15 Mins)
Speaker/Author: Hidayath Ulla (Indian Institute of Technology Kanpur, India); Krishna Manohara (Indian Institute of Technology- Kanpur, India); Pankaj Yadav (Indian Institute of Technology Kanpur, India); Madhu Seetharaman (Indian Institute of Technology- Kanpur, India); Rita Rana and Gopika Pillai (Indian Institute of Technology Kanpur, India); Bodduri Venkata Durga Vijaykumar, Sanjeevkumar Nalluri, Mahesh Kumar Uppada, Saikat Sen and Srinivas Oruganti (Dr Reddys Institute of Life Sciences, India); Muralidharan Balakrishnan (Indian Institute of Technology Kanpur, India); Monica Katiyar (IIT Kanpur, India)
Presenter: Hidayath Ulla

Abstract: To fabricate fully solution-processed small-molecule organic light-emitting diodes (OLEDs), we investigate the slot-die coating technique for the small-molecule electron transport layer (ETL). 2,2′,2"-(1,3,5-Benzinetriyl)-tris(1-phenyl-1-H-benzimidazole) (TPBi) was dissolved in methanol and slot-die coated as ETL and applied in multilayer OLEDs with small-molecule Bis(4-phenylthieno[3,2-c]pyridinato-N, C2') (acetylacetonate) iridium(III) (PO-01) doped in 4,4'- Bis(carbazol-9-yl)biphenyl (CBP) host as an emissive layer. The ETL provides efficient electron injection and electron transport ability in the devices. The efficiency of the devices with the combination of ETL and Ca/Al cathode reaches 0.8 cd/A at 1000 cd/m 2 .

49-4: State of art TADF OLEDs Fabrication Cluster Tool with Novel Charge Transport Layers. (Invited Talk)
Start Time: 05:30 PM (30 Mins)
Speaker/Author: Prof. Dinesh Kabra, Indian Institute of Technology Bombay, India
Presenter: Prof. Dinesh Kabra

Abstract: Organic light emitting diodes (OLEDs) have become a choice of light element for small area display devices and progressing for large area and lighting solutions. With advancement in emissive materials, a lot of emphasize is given to novel thermally activated delayed fluorescence (TADF) based compounds. In general, these devices are multilayer structure with typical thickness of layers in the range of 5nm - 30 nm and require a good control on uniformity and compactness. We developed an indigenous multi-chamber cluster tool to make state-of-art OLEDs, with semi-automation approach. I will share design and results of devices made using this tool which consists of novel charge transport layers for OLED structure with a promise of improved performance in terms of stability and reduced leakage currents.

Session No: 50 | Session Title: Reliability Physics of Semiconductor Devices - 2

Audi: 6 | 04:30 PM-06:00 PM | **Session Chair:** Dr. Pritom Jyoti Bora (SUTD)
Track: Reliability Physics of Semiconductor Devices (RPSD)
Date: 13-Dec-22

50-1: Overview of SER immune Physical IP design (Invited Talk)
Start Time: 04:30 PM (30 Mins)
Speaker/Author: Mr. Anil Kumar Baratam, Arm, Bangalore
Presenter: Mr. Anil Kumar Baratam

Abstract: Radiation induced soft errors are very critical challenges to build Automotive and Infrastructure products. Single Event Upsets could upset multiple circuit nodes in advanced process nodes due to technology scaling. This has captured the increasing interest on SER topic recently.
In this paper, we will discuss about technology scaling of FIT for logic and memory in advanced process nodes. Some of the layout techniques to improve the soft error immunity would be discussed. We will also present

multiple mitigation techniques that can be implemented at register level up to sub-system level such as DCLS, TMR, flipflop hardening, parity, ECC etc.

50-2: Towards reliable circuits using NC/FEFETs (Invited Talk)
Start Time: 05:00 PM (30 Mins)
Speaker/Author: Prof. Anand Bulusu, Indian Institute of Technology Roorkee, Roorkee, India
Presenter: Prof. Anand Bulusu

Abstract: In this talk, we mainly describe our work in understanding the physics of multiple domains, dielectric (DE) phase in FE layer, interface traps in NC/FeFET devices and their impact on circuit reliability. We also discuss the impact of polarization asymmetry in the FE layer due to drain-source voltage in NC/FeFETs. We discuss that the presence of DE phase causes non-uniformity in the polarization and potential contour inside the FE-layer in the gate-dielectric stack. The randomly varying fraction of DE phase, therefore, introduces a higher reliability concern for NC-FETs. In FeFETs, we observe and explain that there exists a certain DE percentage threshold below which the increase of the DE phase does not significantly impact the device memory window. We observe that another reliability issue in NCFETs is caused by the traps at the interfaces of silicon, silicon-di-oxide and hafnium oxide or bulk hafnium oxide traps, which change the FE polarization.

50-3: Listening to Defects via Random Telegraphic Noise (RTN) in nanoscale materials: Scanning Probe Microscopy/spectroscopy studies at room temperature (Invited Talk)
Start Time: 05:30 PM (30 Mins)
Speaker/Author: Dr. Ramesh Mohan Thamankar, Centre for Functional Materials, Vellore Institute of Technology, Vellore, TN, India
Presenter: Dr. Ramesh Mohan Thamankar

Abstract: Extreme scaling of the electronic devices has demanded understanding of materials at nano and atomic scale. The characterization technique used at this level should give details of physical phenomena at nano and atomic scale. Reliability of materials and the devices at this scale will be affected by defects present in the materials used. The discrete and random step wise current jumps will be seen due to the electron capture and emission. In this talk, I will explain the usage of scanning tunneling microscopy/spectroscopy (UHV-STM/STS) for characterizing the materials and understand the defects at nanoscale. Special focus will be given to the random telegraphic noise (RTN) measurements performed on the ALD grown HfO2 which is a very relevant material for the future transistor design point of view.

Session No: 51 | Session Title: Advances in Memory Applications and Modeling

Audi: 7 | 04:30 PM-06:00 PM | **Session Chair:** Prof Daniele Ielmini
Track: Advanced Memory Technologies (AMT)
Date: 13-Dec-22

51-1: Emerging Memory Paradigms from Extreme-Edge to Extreme-Scale Computations (Invited Talk)
Start Time: 04:30 PM (30 Mins)
Speaker/Author: Prof. Akhilesh Jaiswal, University of Southern California-Information Sciences Institute
Presenter: Prof. Akhilesh Jaiswal

Abstract: Memory landscape has dictated the efficiency and speed of computing for decades. The vision to achieve ubiquitous computing spanning edge to cloud has necessitated the need for functional memory technologies that can cater to specific niche of particular computing applications. In this talk, I will discuss two examples of enabling novel computing paradigms spanning extreme-edge to extreme-scale computations driven by recent advances in memory technologies and their monolithic and heterogenous integration schemes. Specifically, the first part of the talk will focus on computer vision applications distributed over edge and cloud using novel memory embedded pixels, while the second part would address a pathway towards ultra-large-scale computing using electro-optic memory solutions.

51-2: Building and Memory Centric World (Invited Talk)
Start Time: 05:00 PM (30 Mins)
Speaker/Author: Prof. Manan Suri, Indian Institute of Technology Delhi, India
Presenter: Prof. Manan Suri

Abstract: We live in an era which is more memory-centric than ever. Factors that contribute to the ever increasing importance of memory are – (i) Saturation of Moore's law, (ii) ease of generating enormous amounts of data and

(iii) exciting new material properties. The nature of present day data intensive applications is such that, excellence in computational performance cannot be achieved alone on the basis of raw transistor scaling or linearly increasing the number of processing cores. A fundamental shift in the vastly successful Von Neumann computational paradigm is needed to overcome the bottlenecks associated with data-intensive real time applications. This is where next generation Non-Volatile Memory (NVM) begins to play a very significant role. Our research group at IIT-D, has been actively working on exploiting the characteristics of emerging NVM nanodevices and nanomaterials for a multitude of novel applications. We have considered emerging technologies such as OxRAM, CBRAM, PCM, RRAM, STT-MRAM etc. building an entire memory-centric application ecosystem comprising of various hybrid CMOS-NVM circuits. Applications realized include: Supervized and Unsupervised Learning (SNNs, CNNs, BNNs), AI Edge-Inference & Training, Sensing, Security, and in-Memory Computing.

51-3: Compact Modelling and Unconventional Applications of 3D NAND Flash Memory (Invited Talk)
Start Time: 05:30 PM (30 Mins)
Speaker/Author: Dr. Shubham Sahay, Indian Institute of Technology Kanpur, India
Presenter: Dr. Shubham Sahay

Abstract: With applications ranging from portable flash drives to SSDs and cloud storage, 3D NAND flash memory has become ubiquitous in this era of internet of things (IoT). However, lack of a proper framework for analyzing the efficacy of 3D NAND flash memory has remained the bottleneck for circuit designers and system architects in this direction. In this talk, we present the first behavioral compact model for 3D NAND flash memory which effectively captures the parasitic coupling components while accurately reproducing the static characteristics. The developed compact model also enables the characterization of stochastic analog behavior. The possibility of exploiting the inherent variability of the 3D NAND flash memory for realizing an adversary-attack resilient strong physical unclonable function (PUF) circuit would also be discussed.

Session No: 52 | Session Title: RF & General MEMS Devices
Audi: 8 | 04:30 PM-05:45 PM | **Session Chair:** Prof. Shanti Bhattacharya
Track: MEMS/NEMS and Heterogeneously Integrated Devices (NEMS)
Date: 13-Dec-22

52-1: Linear and nonlinear effects in 2D Suspended Structures (Invited Talk)
Start Time: 04:30 PM (30 Mins)
Speaker/Author: Prof. Akshay Naik, Indian Institute of Science, Bangalore, India
Presenter: Prof. Akshay Naik

Abstract: Vibrating membranes fabricated using 2D materials are extremely sensitive to various stimuli. In this talk, I'll present our efforts towards using these thin structures as sensors. One of these is a strain sensor fabricating using graphene on a thin silicon diaphragm. These tiny structures vibrate at very high frequencies (10-100MHz) and are exquisitely sensitive to changes in the strain. However, nonlinearities in these devices also constraint their use as linear sensor. In the talk, I'll demonstrate methods for controlling and manipulating these nonlinearities. I'll show how our inability to produce perfect devices leads to nonlinear effects and our ability to control and cancel out nonlinearities leads to enhancement of signal to noise ratio. This regime of near cancellation of the two strongest nonlinearities is not only useful for applications but also to observe higher order nonlinearities and nonlinear damping.

52-2: Measurement of MEMS Actuator Deflection by C-V Method (Oral)
Start Time: 05:00 PM (15 Mins)
Speaker/Author: Satish Kumar Verma (Indian Institute of Technology Delhi, Delhi & IIT Delhi, India); Bhaskar Mitra (IIT Delhi, India)
Presenter: Satish Kumar Verma

Abstract: This study explores the correlation between indirect and direct deflection measurement techniques for MEMS actuators. The measured airgap capacitance is used to calculate deflection using parallel plate model and FEM extracted model for indirect technique. Direct device deflection is measured using an optical profilometer. A 110 μm long and 2.5 μm thick Si-folded cantilever beam with 460 nm airgap electrostatic actuation is used for the measurement. The characterization shows that the device pre-pull-in deflection is up to 98 nm for 4V range with both the methods. The calculated data demonstrate that, in contrast to the parallel plate, which has a 12.7% mean square error, the FEM calibrated model agrees with profilometer to within 8.6% for pre-pull-in deflection.

52-3: MEMS Physical Sensors with Integrated FET based Electromechanical Transduction (Invited Talk)
Start Time: 05:15 PM (30 Mins)
Speaker/Author: Dr. Seena V, Indian Institute of Space Science and Technology (IIST), India
Presenter: Dr. Seena V

Abstract: MEMS sensors and devices have numerous applications spanning across consumer gadgets, automotive electronics, industrial medical, defence, aerospace etc. Despite the wide and increasing demands for MEMS-based devices such as sensors and actuators in diverse applications, unlike semiconductor technologies like CMOS/VLSI, the design and fabrication of MEMS/Microsystems is not fully standardized. Most of the commercially available MEMS sensors are based on passive transduction mechanisms such as capacitive or piezoresistive with inherent performance limitations. FET based active transduction schemes have the potential to overcome these limitations with ease in CMOS-MEMS integration as an additional merit. This talk would give a brief overview of our attempts towards indigenous development of MEMS physical sensors with FET based electromechanical transduction with scope for CMOS-MEMS integration.

Session No: 53 | Session Title: Integrated Photonics - Active devices, Programmability and Nonlinearity
Audi: 9 | 04:30 PM-06:00 PM | **Session Chair:** Prof. Shankar Selvaraja
Track: Integrated Photonics & Fibre Lasers (IPFL)
Date: 13-Dec-22

53-1: Nonlinear optical frequency conversion in multimode adiabatic submicron tapers (Invited Talk)
Start Time: 04:30 PM (30 Mins)
Speaker/Author: Prof. Myeong Soo Kang, Korea Advanced Institute of Science and Technology, Republic of Korea
Presenter: Prof. Myeong Soo Kang

Abstract: I will describe our experimental works on high-efficiency nonlinear optical frequency conversion in multimode nanofibers. We successfully fabricate silica-glass submicron tapers that allow the simultaneous adiabatic transmission of multiple spatial modes. Such multimode adiabatic submicron tapers offer a new opportunity to observe nonlinear and quantum optical effects with unique vectorial properties and implement novel types of multimode photonic quantum information processing. We also demonstrate a widely tunable ultra-narrow-linewidth pulsed laser source suitable for experiments with multimode nanofibers. If time permits, I will also introduce recent efforts to engineer cavity soliton states in a nonlinear fiber resonator, where nonlinear effects other than the Kerr effect are incorporated to alter the conventional Kerr cavity dynamics.

53-2: Programmable Silicon Photonic Circuits (Invited Talk)
Start Time: 05:00 PM (30 Mins)
Speaker/Author: Prof. Wim Bogaerts, Ghent University - IMEC, Belgium
Presenter: Prof. Wim Bogaerts

Abstract: Programmable photonic circuits are chips that manipulate light, and where the flow of light can be configured through a layer of electronics and software. This contrasts strongly with most photonic chips today, which have a fixed flow of light, custom-designed for one application. Programmability on a photonic chip means that the connectivity and functionality can be reconfigured, or even completely synthesized at run time. This is reminiscent of field-programmable gate arrays (FPGA) or digital signal processors (DSP) used in digital electronics. We discuss the basic photonic technology blocks for programmable photonic circuits, and the technological layers around these chips to make them programmable. The programmability in itself significantly lowers the threshold to experiment with photonic circuits, and could accelerate adoption and application developments.

53-3: In-House SiN Process Development for Integrated Photonic Applications (Oral)
Start Time: 05:30 PM (15 Mins)
Speaker/Author: Anushka Tiwari, Sarad Subhra Bhakat, Riddhi Goswami, Pranita Kumari Swain and Arnab Goswami (Indian Institute of Technology Madras, India); Enakshi Bhattacharya (Indian Institute of Technology, Madras, India); Bijoy Krishna Das (Indian Institute of Technology Madras, India)
Presenter: Anushka Tiwari

Abstract: Over the last decade, silicon nitride (SiN) based integrated photonics has become popular due to its CMOS compatibility, low loss, wide spectral operation band and tolerance to high optical power. It has great

potential in different application areas like quantum information processing, microwave photonics, spectroscopy, etc. However, the growth of an optical grade oxide layer (for bottom cladding) and subsequent deposition of SiN device layer on the surface of a handle silicon wafer are the most important aspects for the realization of large-scale photonic integrated circuits with an acceptable waveguide losses and fabrication yields. In this paper, we report the in-house technology development of SiN waveguide devices starting from a 4-inch silicon wafer. Both the thermally grown buried oxide (BOX) and the LPCVD deposited SiN device layer show excellent uniformities in terms of their thickness (1900 ± 20 nm, 400 ± 4 nm, respectively) as well as refractive indices (n SiO2 = 1.45 ± 0.001, n SiN = 2.024 ± 0.003 at $\lambda \sim 1.55\ \mu$m) across the full wafer. We have discussed the design and characterization of the grating coupler, single mode waveguides operating at $\lambda \sim 1.55\ \mu$m and their fabrication flow as well. The fabricated single mode waveguides (TE polarized) with input/output grating couplers exhibit a 3-dB bandwidth of ~ 50 nm with a peak transmission efficiency at $\lambda \sim 1570$ nm. The SiN waveguides fabricated out of in-house processed SiN wafer exhibit reasonable third order non-linearity; confirmed by stimulated four wave mixing experiment.

53-4: Study of Ring-Assisted Mach-Zehnder Interferometer Modulators (Oral)
Start Time: 05:45 PM (15 Mins)
Speaker/Author: Riddhi Nandi (Global Foundries, India); Michal Rakowski (Global Foundries, USA); Avijit Chatterjee and Aneesh Dash (Global Foundries, India); Abdelsalam Aboketaf and Qidi Liu (Global Foundries, USA); Prateek Kumar Sharma (Global Foundries, India)
Presenter: Riddhi Nandi

Abstract: A microring-assisted Mach-Zehnder interferometer has been studied. The structure demonstrates better extinction ratio, eye opening and bandwidth than a single microring modulator. The extinction of the ring-assisted Mach-Zehnder interferometer can be further tailored by controlling the amount of light coupled to each of the interferometer arms. A 7 dB improvement in the extinction ratio over that of a standalone micro-ring device is observed for a 7.54 μm ring radius when operated in over-coupled regime at around 1310 nm wavelength.

Session No: 54 | Session Title: Dense laser integration on silicon
Audi: 10 | 04:30 PM-06:00 PM | **Session Chair:** Prof. Sudharsanan Srinivasan
Track: LED & Semiconductor Lasers: Device, Physics & Modules (LL)
Date: 13-Dec-22

54-1: Heterogeneously integrated InP-laser on Silicon Photonics realized by micro-transfer printing (Invited Talk)
Start Time: 04:30 PM (30 Mins)
Speaker/Author: Dr. Samir Ghosh, Tyndall National Institute, Cork, Ireland
Presenter: Dr. Samir Ghosh

Abstract: Silicon photonics have gained immense commercial interest in data-center market and soon it will enter other domains as well including biomedical, space applications and so on. Silicon being an indirect bandgap semiconductor efficient lasing cannot be achieved. Therefore, hybrid or heterogeneous integration techniques are normally used to incorporate laser with silicon photonics (SiP) platform. These techniques of integrating lasers on SiP platform are far from ideal in-terms of volume, cost and yield. Micro-transfer printing is an emerging technology which enables massively parallel integration with high yield and hence bring the cost down. In this talk transfer printing of InP-based laser on SiP chip will be presented.

Session No: 54 | Session Title: Dense laser integration on silicon
Audi: 10 | 04:30 PM-06:00 PM | **Session Chair:** Prof. Sudharsanan Srinivasan
Track: LED & Semiconductor Lasers: Device, Physics & Modules (LL)
Date: 13-Dec-22

54-2: Integrated silicon photonics with on-chip lasers (Invited Talk)
Start Time: 05:00 PM (30 Mins)
Speaker/Author: Prof. Yating Wan, KAUST
Presenter: Prof. Yating Wan

Abstract: Integrated Si photonics has sparked a significant ramp-up of investment in both academia and industry as a scalable, power-efficient, and eco-friendly solution. At the heart of this platform is the light source, which has been the focus of research extensively. This talk tries to tackle this issue from two perspectives: heterogeneous

integration based on wafer bonding and monolithic integration based on direct epitaxial growth. We will talk about the current state of application-driven on-chip silicon lasers. We expect to inspire further development in incorporating photonic integrated circuits with on-chip lasers for substantial performance gains, green solutions, and mass production.

54-3: Photonic Integrated Circuits using an open market silicon photonics PDK with integrated lasers (Invited Talk)
Start Time: 05:30 PM (30 Mins)
Speaker/Author: Dr. Anand Ramaswamy, Openlight Photonics, USA
Presenter: Dr. Anand Ramaswamy

Abstract: This talk will review the world's first open silicon photonics platform with integrated lasers to enable the design of PICs for datacom and sensing applications. OpenLight's III-V-on-SOI technology is currently offered by Tower Semiconductor in a PDK whose component library includes InP-based lasers, semiconductor optical amplifiers, high-speed modulators and detectors; as well as a wide range of state-of-the-art passive silicon components to form a complete solution for low-power, high-performance photonics integrated circuits.

Session No: 55 | Session Title: Emerging memories for Neuromorphic Computing
Audi: 11 | 04:30 PM-06:00 PM | **Session Chair:** Prof. Sandip Mondal
Track: Neuromorphic Device Technology, Circuits and Systems (NDTCS)
Date: 13-Dec-22

55-1: Uncovering stochastic write-error problems in STT-MRAM using micromagnetic modeling (Invited Talk)
Start Time: 04:30 PM (30 Mins)
Speaker/Author: Prof. Tanmoy Pramanik, Indian Institute of Technology Roorkee
Presenter: Prof. Tanmoy Pramanik

Abstract: Successful demonstrations of STT-MRAM prototypes in recent years have shown promising performance and reliability for embedded non-volatile memory applications. However, sub-nanosecond switching required for cache applications often is hindered by anomalous write error issues. In this talk, I'll discuss how micromagnetic modeling can help to understand the root cause of such problems. Another lingering issue is how the magnetic memory behaves in presence of external magnetic field perturbation. I'll share our modeling results that, for the first time, show how the write error variations in the presence of an external magnetic field can hamper memory operation and impact magnetic immunity.

Session No: 55 | Session Title: Emerging memories for Neuromorphic Computing
Audi: 11 | 04:30 PM-06:00 PM | **Session Chair:** Prof. Sandip Mondal
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55-2: Experimental Demonstration of VO2 Based Lateral/Vertical Devices and Relaxation Oscillator With an Ultra-Low Thermal Budget Process (Oral)
Start Time: 05:00 PM (15 Mins)
Speaker/Author: Ashok P (Indian Institute of Technology Kanpur, India); Yogesh Chauhan (IIT Kanpur, India); Amit Verma (Indian Institute of Technology Kanpur, India)
Presenter: Ashok P
Abstract: Vanadium dioxide (VO2) has been exploited in steep subthreshold slope switches, coupled oscillators for neuromorphic computing, and selectors for RRAM due to its intrinsic insulator to metal phase transition properties. The thin-film synthesis of VO2 needs a high-temperature process or long annealing duration, which increases the thermal budget and is difficult to integrate with the back-end of line CMOS technology process. In this work, we use a low thermal budget process to fabricate and characterize both horizontal and vertical VO2 devices. In both configurations, VO2 devices show voltage induced reversible switching beyond a threshold voltage. The threshold voltage of devices decreases monotonically as a function of decreasing channel length of the devices. The vertical device shows the lowest threshold voltage compared to the horizontal structure due to significantly smaller channel length. Finally, we demonstrate a relaxation oscillator using the fabricated VO2 devices which shows stable oscillations over half a million cycles with an oscillation frequency of 1.75 kHz. We also demonstrate voltage-controlled tuning of the oscillation frequency in the range of ~1.3-2 kHz. This demonstration of VO2 devices with a low-thermal budget process will be helpful for integrating VO2-based phase transition devices with CMOS technology.

55-3: Neuromorphic Accelerator for Deep Spiking Neural Networks With NVM Crossbar Arrays (Oral)
Start Time: 05:15 PM (15 Mins)
Speaker/Author: Shruti Kulkarni (Oak Ridge National Laboratory, USA); Shihui Yin and Jae-sun Seo (Arizona State University, USA); Bipin Rajendran (King's College London, United Kingdom (Great Britain))
Presenter: Shruti Kulkarni

Abstract: In this paper, we present a scalable digital hardware accelerator based on non-volatile memory arrays capable of realizing deep convolutional spiking neural networks (SNNs). Our design studies are conducted using a compact model for spin-transfer torque random access memory (STT-RAM) devices. Large networks are realized by tiling multiple cores which communicate by transmitting spike packets via an on-chip routing network. Compared to an equivalent SRAM based core design, we show that the STT-RAM based design achieves nearly 15X higher GSOPS (Synaptic Operations per Second) per Watt per mm 2 making it a promising platform for realizing systems with significant area and power limitations.

55-4: Two-Dimensional Material-based Higher-Order Neuromorphic Computing with Dynamic Weights (Invited Talk)
Start Time: 05:30 PM (30 Mins)
Speaker/Author: Prof. Amit Ranjan Trivedi, University of Illinois at Chicago
Presenter: Prof. Amit Ranjan Trivedi

Abstract: The increasing complexity of deep learning systems has pushed conventional computing technologies to their limits. While memristor is one of the prevailing technologies for deep learning acceleration, it is only suited for classical learning layers where two operands, namely weights and inputs, are processed at a time. Meanwhile, to improve the computational efficiency of deep learning for emerging applications, a variety of non-traditional layers, requiring concurrent processing of many operands, are becoming popular. For example, hypernetworks improve their predictive robustness by simultaneously processing weights and inputs against the application context. Two-electrode memristor grids cannot natively support such operations of emerging layers. Addressing the unmet need, this talk discusses two-dimensional material-based neuron and synapses that can be controlled by multiple gate terminals. Thus, exploiting crossbar's gate controllability, multiple operands could be concurrently processed within the same crossbar. Many advanced inference architectures that can generalize beyond a typical passive crossbar thus become possible. Overall, the ultra-low-power, higher-order processing capacity of the discussed gate-tunable crossbars and neurons harnesses high robustness and efficiency of emerging deep learning layers within area/power-constrained devices such as mobile, sensor, and embedded systems.

Session No: 56 | Session Title: Growth and application of 2D materials

Audi: 1 | 11:15 AM-01:00 PM | **Session Chair:** Prof. Saptarshi Das
Track: 2D Material Based Technologies (2DT)
Date: 14-Dec-22

56-1: Lateral Band Engineering in Two-Dimensional Heterostructures and Devices (Invited Talk)
Start Time: 11:15 AM (30 Mins)
Speaker/Author: Prof. Prasana Kumar Sahoo, Indian Institute of Technology Kharagpur, India
Presenter: Prof. Prasana Kumar Sahoo

Abstract: 2D heterostructures possess fascinating physical properties and emerging applications. We demonstrated the direct growth of multi-junction MoX2-WX2 (X= Se/S) lateral heterostructures and their alloys (Nature 2018, ACS Nano 2019, Small 2022). The extent of the spatial modulation of individual TMD domains and their optical and electronic transition characteristics across the heterojunctions are studied in detail. Temperature-dependent photoluminescence study further provides a better understanding of the optical properties of these heterostructures. Electrical transport measurements revealed the formation of multiple 2D PN junctions/diodes that showed pronounced photo-sensing, photovoltaic, and electroluminescence characteristics. The role of several intrinsic and extrinsic factors in the performance of these 2D devices will also be discussed.

56-2: Spatially Controlled Growth of 2D Materials (Invited Talk)
Start Time: 11:45 AM (30 Mins)
Speaker/Author: Prof. Zakaria Al Balushi, University of California, Berkeley
Presenter: Prof. Zakaria Al Balushi

Abstract: The surface potential of graphene can be modulated with strain and doping by engineering the underlaying sub-surface in which the graphene resides on. Here we discuss a detailed investigation to correlate

the influence of the underlying sub-surface on modulating the surface potential of graphene on a diamond like carbon (DLC) substrate through a heterointerface containing trapped gallium in uniquely designed spatial structures. Through our heterointerface engineering approach of the graphene surface potential landscape, we show selective area growth of 2D materials on the graphene surface . This study will provide a deep understanding on the influence of graphene surface potential on the nucleation and surface diffusion process for the growth of chalcogenide 2D semiconductors.

56-3: Large Purcell Enhancement in Monolayer MoSe2 Flakes Using Ga Nanodroplets (Oral)
Start Time: 12:15 PM (15 Mins)
Speaker/Author: Durgesh Banswar (IIT Delhi, India)
Presenter: Durgesh Banswar

Abstract: Plasmonic effects in metal nanoparticles enhancing near-field light-matter interaction have multiple applications in bright sources and sensing. Gallium (Ga) is an important plasmonic material allowing for flexible electronics with facile room-temperature synthesis and tunable resonances in visible spectrum range. Here, in addition to showing a three-fold near-field plasmonic enhancement observable in Raman spectroscope, we demonstrate a spectrally selective strong Purcell enhancement of the B-exciton series in chemically synthesized MoSe2 flakes.

56-4: Fundamentals of thermoelectric engines with twisted 2D bilayers of graphene (Invited Talk)
Start Time: 12:30 PM (30 Mins)
Speaker/Author: Prof. Arindam Ghosh, Indian Institute of Science
Presenter: Prof. Arindam Ghosh

Abstract: Thermoelectricity is an unconventional but extremely sensitive probe to the effects of electronic interactions in solids. Thermoelectric measurement often complements standard electrical transport and detects electronic correlations through departure from the well-established Mott semiclassical framework. Recent emergence of twisted bilayers of graphene provides a new versatile platform to explore not only several fundamental aspects of thermoelectricity at the atomic scale, but also design a new class of thermoelectric devices. I shall present how thermoelectricity can probe the inter-layer coupling in twisted bilayers, and exploit the understanding in realizing a unique class of heat engines.

Session No: 57 | Session Title: Photovoltaic Reliability

Audi: 2 | 11:15 AM-01:00 PM | **Session Chair:** Prof. Anil Kottantharayil
Track: Solar Cells & Photodetectors: Physics, Device, & Modules (SP)
Date: 14-Dec-22

57-1: Impact of Halide Ion Migration on the Stability of Perovskite Solar Cells (Invited Talk)
Start Time: 11:15 AM (30 Mins)
Speaker/Author: Prof. Prashant V. Kamat, University of Notre Dame
Presenter: Prof. Prashant V. Kamat

Abstract: The intrinsic ionic defects, specifically halide ion vacancies, often dictate the mobility of halide species within the metal halide perovskite film during the operation of solar cells. Of particular interest is the halide ion mobility in mixed halide perovskites, which offer an insight into the halide ion migration. The origin of processes leading to halide migration is investigated using mixed halide perovskite films. Both hole trapping at I-site and the defect mediated migration influence the mobility of iodide species under photoirradiation. The iodide species migrating toward the grain boundaries render the mixed halide film phase-segregated under photoirradiation. Ways to suppresses the halide ion mobility through introduction of Cs at the A-site will be discussed.

57-2: Comparison of Polymeric and Metal Oxide Hole Transport Material on the Stability of FASnI3 Perovskite Solar Cell (Oral)
Start Time: 11:45 AM (15 Mins)
Speaker/Author: Basavaraju U (Indian Institute of Science & Central Manufacturing Technology Institute, India); Bidisha Nath (Indian Institute of Science, India); Naga Hanumaiah (Central Manufacturing Technology Institute, India); Praveen C Ramamurthy (Indian Institute of Science, India)
Presenter: Basavaraju U

Abstract: The Tin-based perovskite is an encouraging material in the development of non-toxic solar cell application, but its performance is limited by the poor chemical stability against oxygen and moisture. Therefore,

tin-based perovskite solar cells are mostly fabricated in inverted planar device structures and the selection of underlying hole transport material plays a significant role in device stability. In this work, we report the comparison study between a metal oxide, nickel oxide, and polymeric poly(3,4-ethylenedioxythiophene): poly(styrenesulfonate) (PEDOT: PSS) as a hole transport layer on device efficiency and stability of tin-based PSC. We obtained comparatively higher power conversion efficiency (PCE) with NiOx than others, however, the solar cell with PEDOT: PSS is more stable rather than NiOx for the duration of 900 hrs in a nitrogen ambient, without encapsulation.

57-3: Development of Roll-To-Roll Coated ZIF-67-Modified on PET as an Emerging Encapsulant for Photovoltaics (Oral)
Start Time: 12:00 PM (15 Mins)
Speaker/Author: Jinu Joji and Varun Adiga (Indian Institute of Science, India); Luke Sutherland and Hasitha Weerasinghe (CSIRO, India); Praveen C Ramamurthy (Indian Institute of Science, India)
Presenter: Jinu Joji

Abstract: Polyethylene terephthalate (PET) substrates were modified with a metal-organic framework for the fabrication of an encapsulant film. Zeolitic imidazolium framework (ZIF- 67) was dispersed in a polyvinyl alcohol (PVA) matrix which was then used for the roll-to-roll coating over the PET sheet. The moisture barrier properties were evaluated using cavity ring-down spectroscopy (CRDS). The water vapor transmission rate obtained was ~ 0.26 g/m2/day. About > 45 times improvement in the moisture barrier and excellent optical transmittance properties were observed for the post-modified ZIF- 67|PET compared to the bare PET.

57-4: Data-Driven Approach for Quantifying the Risk of Hail Impact on Photovoltaic Plants (Oral)
Start Time: 12:15 PM (15 Mins)
Speaker/Author: Sayli A Bhavsar and Narendra Shiradkar (Indian Institute of Technology Bombay, India)
Presenter: Sayli A Bhavsar

Abstract: This paper presents an approach for quantifying the risk associated with hail storms on Photovoltaic plants using the data provided by the Storm Prediction Center of the National Oceanic and Atmospheric Administration, USA. Limits of existing accelerated tests in IEC 61215 to simulate hail impact are quantified and advantages of more severe accelerated tests are quantified for a selected location in the US which is prone to hail storms and is also home to large PV plants. Moreover, various data-mining based approaches for generating a reasonable quality hail size and frequency data for India are explored and their limitations are identified.

57-5: Desert Photovoltaics - Performance and reliability issues of PV modules in hot climatic conditions (Invited Talk)
Start Time: 12:30 PM (30 Mins)
Speaker/Author: Dr. Jim Joseph John, R&D center, Dubai Electricity and Water Authority (DEWA), UAE
Presenter: Dr. Jim Joseph John

Abstract: The photovoltaic industry has reached a major milestone of installed global capacity of 1TW. The desert regions are ideal locations for installing large power plants. However, the expectations of PV system operating for 20-30 years or more can be challenging due to the harsher climatic conditions. Therefore, improving the risk associated with weather-induced degradation of PV modules will reduce uncertainity in lifetime energy production, which in turn reduces financial risk and improves financing opportunities for projects located in these regions. In this talk, I will be sharing the degradation issues of different PV module types located in the 5GW MBR Solar park. The climate severity will be discussed, followed by its impact on the PV module BOM will be shown. Requirement for climate specific qualification standards and module design will be explored.

Session No: 58 | Session Title: WBG device based integrated systems and application considerations

Audi: 3 | 11:15 AM-01:00 PM | **Session Chair:** Mr. Yoganand Parthasarathy
Track: Wide Bandgap Device Based Circuits and Systems (WDCS)
Date: 14-Dec-22

58-1: Exploring the Feasibility of AlN/GaN HEMTs for THz Applications Using a Novel Device-Circuit Co-Design Approach (Oral)
Start Time: 11:15 PM (15 Mins)
Speaker/Author: Harsha B Variar (Indian Institute of Science, India); Ajay Singh (Indian Institute of Science Bangalore, India); Ankit Soni (Indian Institute of Science, India); Mayank Shrivastava (Indian Institute of Science Bangalore, India)
Presenter: Harsha B Variar

Abstract: This work presents a rigorous device-circuit co-design investigation of AlN/GaN HEMT to explore its feasibility for operations at frequencies ~1 THz. A novel device-circuit co-design methodology was adopted, which involves I-V/C-V/S-parameter matching, careful extraction of a small signal model and large-signal model. This was followed by source-load pull-based power amplifier (PA) design/exploration as a function of various device design parameters. For PA operation, both class–A and class–AB operations were invested while exploring PA gain, output power, efficiency at 1dB compression point, and linearity through dual-tone (IMD3) investigations. A complete range of device design parameters are evaluated to explore the ultimate scalability limit of AlN/GaN HEMT for possible THz operation. A correlation between the device's intrinsic parameters and PA performance has also been established to uncover AlN/GaN HEMT's feasibility for ~1 THz active operation.

58-2: Powering a sustainable future – Two important vectors enabling next-generation of energy efficient power management ICs (Invited Talk)
Start Time: 11:30 AM (30 Mins)
Speaker/Author: Dr. Raveesh Magod, Texas Instruments, USA
Presenter: Dr. Raveesh Magod

Abstract: Power management has been a key enabler for a variety of ever increasing modern day electronic applications like smartphones, data center servers, electric vehicles and smart grids to name a few. However, in order to achieve climate neutrality targets and also cater to surging energy consumption by such applications across the globe, it is imperative that such solutions need to be highly efficient. This talk focuses on wide-bandgap (GaN and SiC) based converters and ultra-low quiescent power converters, which are identified as two key directions for next-generation of sustainable power management ICs that achieve higher energy efficiency. Insights into latest industry products, ongoing research and future trendlines are discussed in detail.

58-3: Characterisation and Modelling of the Switching transitions of WBG Devices (Invited Talk)
Start Time: 12:00 AM (30 Mins)
Speaker/Author: Prof. Kaushik Basu, Indian Institute of Science
Presenter: Prof. Kaushik Basu

Abstract: Silicon Carbide MOSFETs (SiC MOSFETs) fall into the class of wide band gap (WBG) power devices. These devices are commercially available in the voltage range of 600-3300V and compete with the state-of-the-art Si-insulated gate bipolar junction transistors (IGBTs). Superior material properties of SiC MOSFET lead to smaller die sizes. This results in faster switching transients and lower switching loss. However, it excites device and circuit parasitic that may lead to prolonged oscillation, high device stress, spurious turn-on and EMI-related issues. So, the benefit of using SiC MOSFET as a power device comes with numerous design challenges resulting in slow commercial adaptation. It is predicted that the overall market share of WBG devices (SiC and GaN together) will be roughly 10% of the total market for power semiconductors by 2025. To overcome the design challenges and fully utilise the benefits of fast-switching SiC MOSFETs, a better understanding of switching dynamics is essential. However, the switching dynamics of SiC MOSFET are different compared to its Si counterpart due to the highly non-linear device characteristics and participation of circuit parasitic in the process. In this talk, we will discuss our recent work on developing an analytical model of the switching dynamics for hard and soft transitions of SiC MOSFET by simplifying the complex non-linear dynamics predicted by the behavioural model. The developed model, given the device-related parameters extracted from the data sheet, estimated or measured circuit parasitic, can predict lost switching energy, rate of change of device voltage etc., necessary for a successful power converter design through computation with sufficient accuracy.

58-4: Indigenous GaN MMIC Technology (Invited Talk)
Start Time: 12:30 PM (30 Mins)
Speaker/Author: Dr. Meena Mishra, Drdo,India
Presenter: Dr. Meena Mishra

Abstract: Future trends for next generation strategic systems require multifunctionality and modularity like combining radar, communications, and electronic warfare in one system. This higher level of functional integration improves system performance through heightened awareness, improved responsiveness, and mission execution. The use of gallium nitride (GaN) MMIC as key component enables higher performance of systems meeting the requirements in small size with high power and hence GaN MMIC are emerging as an alternative or replacement for laterally diffused MOSFET (LDMOS) components. In most of next generation systems GaN MMIC technology is being considered because of high power density, high efficiency, wide bandwidth, and exceptionally long life. GaN on SiC has superior properties like higher breakdown voltage; higher saturated electron drift velocity and higher thermal conductivity. Hence GaN HEMTs also offer greater power density and

wider bandwidths compared to Si; GaAs; and GaN on Si transistors. As shorter gate length GaAs and GaN transistors become available, coupled with improved circuit design techniques, new devices are becoming available that can perform comfortably to millimeter wave frequencies, opening new applications that were hard to contemplate a decade ago. This paper will briefly describe the indigenous GaN semiconductor technology that is enabling these developments to achieve optimum performance of devices, circuits and subsystems based on this technology.

Session No: 59 | Session Title: Heterogenous Integration : Chiplets and 3D
Audi: 4 | 11:15 AM-01:00 PM | **Session Chair:** Dr. Rama Divakaruni
Track: Advanced Logic Technologies (ALT)
Date: 14-Dec-22

59-1: Electro-Thermal Signoff For Next Generation 3DICs (Invited Talk)
Start Time: 11:15 AM (30 Mins)
Speaker/Author: Mr. Vinayakam Subramanian, Ansys, India
Presenter: Mr. Vinayakam Subramanian

Abstract: This topic will cover the importance of using simulation to address key challenges in semiconductor 3DIC design. Semiconductors/ICs are now the backbone of many industries, ranging across computing (microprocessors, GPUs), telecommunication (smartphones), household appliances (sensors, Internet of Things devices), transportation. This presentation will highlight how simulation is key to designing ICs for such complex applications, while addressing time to market, power consumption, performance and area/size constraints. Specifically, the presentation will focus on the evolution of IC design from single wafers to 3DIC structures and the complexities associated with power integrity, signal integrity and thermal analysis of such advanced designs. We will discuss simulation workflows covering input data and modelling requirements, while also looking at key simulation results that can enable design closure.

59-2: Chipletization and the Power of Heterogeneous Integration (Invited Talk)
Start Time: 11:45 AM (30 Mins)
Speaker/Author: Prof. Madhavan Swaminathan, Georgia Institute of Technology, USA
Presenter: Prof. Madhavan Swaminathan

Abstract: The semiconductor industry is headed towards heterogeneous integration through the dense connectivity of chiplets driven by the high cost of monolithic integration, extended time to market using advanced process nodes on large designs, and emerging heterogeneity of systems.
After providing a brief introduction into the reasons why heterogeneous integration using semiconductor packaging is a means to continue Moore's law, I will present on some of our recent advances and contributions in System on Package (SoP) technologies, a concept that we have been pioneering for almost three decades, that has relevance to emerging applications in Artificial Intelligence, and Wireless Communications.

59-3: Accelerated Modeling for Design Space Exploration of Heterogeneously Integrated Systems: Is Machine Learning Useful? (Invited Talk)
Start Time: 12:15 PM (30 Mins)
Speaker/Author: Prof. Ganesh Subbarayan, Purdue University, USA
Presenter: Prof. Ganesh Subbarayan

Abstract: Modeling for design space exploration of Heterogeneously Integrated (HI) systems is well understood as a multi-physics problem but is less commonly recognized as a multi-scale problem. In this talk we systematically explore (1) adaptive grid solution strategies for systematic trade-off between solution accuracy and computational speed, (2) decomposition of problem domain to enable compact models of sub-domains [3] and to enable a coordinated multi-level analysis, (3) machine learning models as compact models of decomposed domains, and (4) the computational cost of training and using machine learning models relative to physical models. We will conclude with potential strategies for the efficient design exploration of HI systems including Physics Informed Neural Networks (PINNs).

59-4: Safety and Proper Selection of Gas Delivery Systems for Semiconductor Industry (Sponsored)
Start Time: 12:45 PM (15 Mins)
Speaker/Author: Mr. Joerg Koch, Semicon Tech
Presenter: Mr. Joerg Koch

Abstract: Having a reliable gas delivery system is imperative for semiconductor manufacturing industries. The manufacturing process involves the efficient use of over thirty different gases—one of the broadest range of gases used for any industry—to shape a semiconductor's electrical properties at the molecular level. Some of the gases involved include Chlorine, Boron Trichloride, Silane, Ammonia & Nitrous Oxide. These gases need to be precisely applied at each step of the manufacturing process to produce desired reactions. Understanding the role of gases helps manufacturers acknowledge the importance of a reliable gas delivery system in semiconductor fabrication.

Session No: 60 | Session Title: Sustainable Devices and Systems
Audi: 5 | 11:15 AM-01:00 PM | **Session Chair:** Prof. Cantarella Giuseppe
Track: Macroelectronics & Displays: Devices, Circuits & Systems (DIS)
Date: 14-Dec-22

60-1: Sustainable Materials and Design Approaches for Soft Electronics and Robotics (Invited Talk)
Start Time: 11:15 AM (30 Mins)
Speaker/Author: Prof. Martin Kaltenbrunner, Department of Soft Matter Physics, Johannes Kepler University Linz
Presenter: Prof. Martin Kaltenbrunner

Abstract: Modern societies rely on a multitude of electronic and robotic systems, with emerging stretchable and soft devices enabling ever closer human machine interactions. These advances however take their toll on our ecosystem, with high energy demand, greenhouse gas emission and environmental pollution.
Mitigating some of these adverse effects, this talk introduces materials and methods for soft systems that biodegrade. Based on highly stretchable biogels and degradable elastomers, our forms of soft electronics and robots are designed for prolonged operation in ambient conditions without fatigue, but fully degrade after use through biological triggers. Electronic skins provide sensory feedback. 3D printing of biodegradable hydrogels enables omnidirectional soft robots with multifaceted optical sensing abilities. Enabling autonomous operation, stretchable and biodegradable batteries are introduced that power wearable sweat sensors.

60-2: Sustainable Electronic Materials and Devices (Invited Talk)
Start Time: 11:45 AM (30 Mins)
Speaker/Author: Prof. Shweta Agarwala, Aarhus University
Presenter: Prof. Shweta Agarwala

Abstract: Sustainability and health are two of the global challenges recognized by UN. Electronics is the pillar that supports the innovation in these sectors. However, current electronic components are non-biodegradable and release toxins in environment, while the implanted electronics is not compatible with soft human tissues. The aim of my research is to overcome these challenges through i) development of novel electronic material library, and ii) next-generation devices with new form factors. Through green chemistry we have developed novel biodegradable, biocompatible and bioresorbable electronic materials. Printed electronics is the new emerging fabrication technique that allows electronic components, circuits and devices to be put on a desired surface using nanoparticle inks. The synthesized materials are converted into printable inks to fabricate soft and flexible devices. I will showcase some of the case studies on the application of the materials and flexible devices.

60-3: Flexible Organic Transistors With Hybrid Gate Dielectric Consisting Albumen as an Edible Component (Oral)
Start Time: 12:15 PM (15 Mins)
Speaker/Author: Gargi Konwar, Sachin Rahi and Shree Prakash Tiwari (Indian Institute of Technology Jodhpur, India)
Presenter: Gargi Konwar

Abstract: Flexible electronics utilizing emerging edible natural materials as device components lead a path towards the development of cost-effective, renewable, sustainable, and eco-friendly smart systems. Here, an edible and natural biopolymer egg albumen was explored with a thin high-k HfO2 layer to form a hybrid gate dielectric layer for the demonstration of flexible organic transistors. The thin high-k dielectric layer enables the devices to be operated at low voltage while the biopolymer layer helps in forming a better dielectric semiconductor interface. The fabricated devices have shown excellent p-channel characteristics at a low operating voltage of -5 V. Moreover, these devices exhibited good electrical and operational stability to be used in practical applications. These findings suggest that this proposed gate dielectric combination can be an interesting and potential component for flexible organic devices.

60-4: Solution-based Organic Thin Film Transistor Technology Towards Circuits: Challenges and Possible Solutions (Invited Talk)
Start Time: 12:30 PM (30 Mins)
Speaker/Author: Dr. Soumya Dutta, Indian Institute Of Technology Madras, India
Presenter: Dr. Soumya Dutta

Abstract: Substantial progress in organic thin film transistor (OTFT) has emerged the possibilities of realizing analog circuit applications such as low frequency amplifier for sensors, backplane circuits for flexible display, image sensors etc. Going forward, a number of scientific and technological challenges need to be addressed. Scalable manufacturing of OTFTs on polymer dielectric is one of the foremost challenges to make the technology sustainable. While scaling down the size, contact effect becomes the predominating factor deteriorating the device and circuit performances. Our research group actively involves in the development of solution based all-organic thin film transistors adapting microelectronic technology especially photolithography techniques to realize miniaturized high resolution device structure. In this presentation, our recent results on the technological aspects of scalable production of OTFT and alleviation of contact effect especially in solution-processed technology will be demonstrated.

Session No: 61 | Session Title: Quantum Control & Cryogenic Electronics

Audi: 6 | 11:15 AM-01:00 PM | **Session Chair:** Dr. Amith Singhee (IBM)
Track: Quantum Control & Cryogenic Electronics (QCCE)
Date: 14-Dec-22

61-1: Photonic quantum state engineering for secure quantum communication (Invited Talk)
Start Time: 11:15 AM (30 Mins)
Speaker/Author: Prof. Bhaskar Kanseri, Indian Institute of Technology Delhi, India
Presenter: Prof. Bhaskar Kanseri

Abstract: Engineered photonic quantum states of light find applications in developing quantum technologies such as quantum communication. One well known example is quantum key distribution (QKD), which utilises the principles of quantum mechanics and has become a new generation security solution that does not rely on the computation assumptions of problems presumed difficult. This talk would highlight efforts being made by our group at IIT Delhi for both research and development in photonic quantum technologies. Some implementations of QKD in lab scale and in field settings would be discussed. The prospects of photonic quantum technologies would also be highlighted leading to future secure quantum internet.

61-2: Control Challenges for State-of-the-art Quantum Computing (Sponsored)
Start Time: 11:45 PM (15 Mins)
Speaker/Author: Mr. Nitin Nigam, Keysight Technologies
Presenter: Mr. Nitin Nigam, Keysight Technologies

Abstract: Key discussion of paper will be on various Control challenges and Introduction of High-performance Control Systems for Advance Quantum Computing.

61-3: An all-electronic true random number generator (Invited Talk)
Start Time: 12:00 PM (30 Mins)
Speaker/Author: Prof. Kausik Majumdar, Indian Institute of Science, India
Presenter: Prof. Kausik Majumdar

Abstract: Generators of random sequences used in cryptographic applications rely on entropy sources for their indeterminism. Physical processes governed by the laws of quantum mechanics are excellent sources of entropy available in nature. However, the read-out from such systems for generating truly random sequences is challenging while maintaining the feasibility of the extraction procedure for real-world applications. I shall present an all-electronic van der Waals heterostructure-based device generating a random sequence with record-high value (>0.98 bits/bit) of min-entropy through the detection of discrete charge fluctuation in a quantum dot embedded in a tunnel junction. The generated high quality random sequence passes tests such as NIST SP 800-90B and NIST SP 800-22.

61-4: Hybridization in Plasmonic Devices: a path to outperform their Si Counterparts (Invited Talk)
Start Time: 12:30 AM (30 Mins)
Speaker/Author: Prof. Amr S Helmy, University of Toronto
Presenter: Prof. Amr S Helmy

Abstract: For integrated optical devices and resonators, realistic utilization of the superior wave-matter interaction offered by plasmonics is typically impeded by Ohmic loss, which increase rapidly with mode volume reduction. Although coupled-mode plasmonic structures have demonstrated effective alleviation of the loss-confinement trade-off, stringent symmetry requirements must be enforced for such reduction to prevail. In this work, we report an asymmetric plasmonic waveguide that is not only capable of guiding subwavelength optical mode with long-range propagation, but is also unrestricted by structural, material, or modal symmetry. In these composite hybrid plasmonic waveguides (CHPWs), the versatility afforded by the coupling dissimilar plasmonic modes allow better fabrication tolerance and provide more degrees of design freedom to simultaneously optimize various device attributes. Specifically, experimental realization of CHPW demonstrates propagation loss and mode area of only 0.03 dB/μm and 0.002 μm2 respectively, corresponding to the smallest combination amongst long- range plasmonic structures reported to-date. As these waveguide attributes are robust over large process conditions and optical bandwidth, CHPW ring resonator with 2.5 μm radius has been realized with record Purcell factor compared to existing plasmonic and dielectric resonators of similar radii.
Using this platform, record experimental attributes such as normalized Purcell factor approaching 104, 10-dB amplitude modulation extinction ratio with <1 dB insertion loss and fJ-level switching energy, and photodetection sensitivity and internal quantum efficiency of -54 dBm and 6.4 % respectively have been realized within our amorphous-based, CHPW. The ability to support multiple optoelectronic phenomena while providing performance gains over existing plasmonic and dielectric counterparts offers a clear path towards reconfigurable, monolithic plasmonic circuits.

Session No: 62 | Session Title: On-Chip ESD Devices and Physics

Audi: 7 | 11:15 AM-01:00 PM | **Session Chair:** Harshit Dhakad (Intel)
Track: Electrostatic Discharge Reliability (ESD)
Date: 14-Dec-22

62-1: On-chip System level IEC ESD protection issues in Automotive Ics (Invited Talk)
Start Time: 11:15 AM (30 Mins)
Speaker/Author: Dr. Kranthi Nagothu, Texas Instruments, India
Presenter: Dr. Kranthi Nagothu

Abstract: In this talk, unique failure mechanisms in high voltage Silicon Controlled Rectifiers (SCR) under IEC stress are discussed. In one case, the presence of a common mode choke in the stress path was found to change the current waveform shape that the electrostatic discharge (ESD) protection device experiences on-chip. Minor variations in the stress current waveform shape for specific IEC stress levels are found to cause an unexpected window failure in DeNMOS based SCR. In second, Air-Discharge IEC failure in Bi-Directional SCRs that are sensitive to IEC measurement conditions via the pulse rise time are investigated. 3D-TCAD simulations are used to develop the physical Insights of the failure and propose the device level engineering solutions to mitigate the IEC failures.

62-2: Physical Insights Into the ESD Behavior of Field Plated UHV LDMOS Devices (Oral)
Start Time: 11:45 PM (15 Mins)
Speaker/Author: Harsha B Variar (Indian Institute of Science, India); Jhnanesh Somayaji (Srinivasnagar, India); Mayank Shrivastava (Indian Institute of Science Bangalore, India)
Presenter: Harsha B Variar

Abstract: Field plates are commonly used to extend the breakdown voltage to achieve high voltage devices. But, the role of field plates in the ESD behaviour of these devices is still not addressed. This work provides physical insights into the ESD behaviour of field plated Ultra High Voltage Laterally Diffused Metal Oxide Semiconductor (UHV LDMOS) devices. UHV devices are simulated and compared using 3D TCAD simulations. For the first time, the role of field plates in ESD design aspects is investigated. This paper highlights the importance of each field plate (Gate Field plate (GFp), Source Field plate (SFp) and Drain Field plate (DFp)), exploring their individual roles. It was found that GFp and SFp play a significant role in improving the trigger voltage and holding voltage, while DFp is the sole reason for enhancing the failure threshold. Finally, a 3D device failure study is performed to support the theory drawn from 2D simulations.

62-3: The Physical Insight Into Holding Voltage Engineering of SCR for ESD Protection (Oral)
Start Time: 12:00 PM (15 Mins)
Speaker/Author: Satendra Kumar Gautam and Jatin Jatin (Indian Institute of Science, India); M. Monish Murali (Indian Institute of Science Bangalore, India); Mayank Shrivastava (Indian Institute of Science, India)
Presenter: Satendra Kumar Gautam

Abstract: In this work, the holding voltage characteristics of Silicon-Controlled-Rectifier (SCR) with different cathode structures are studied and compared. The cathode structures include the different W/L ratios and the gap between the P+ and N+ diffusion layers (pocket implants) in the cathode Pwell region. These devices show tunable high holding voltage and improved failure current (It2), which strongly depends on the W/L ratio of P+ and N+ diffusion layers. The uniform carrier current distribution in the cathode allows tuning holding voltage with W/L > 1 without affecting the other TLP characteristics like breakdown voltage, trigger voltage, depth of snapback, and holding current. With a higher W/L ratio >1, the failure current can be improved significantly by 30%. Hence, this work provides physical insights into the holding voltage and failure current engineering in high holding voltage (HHV) SCRs, which offers a robust design for Electrostatic Discharge (ESD) protection.

62-4: Performance and Reliability Co-Design of HV Devices in Vertically Stacked Nanosheet Technology (Oral)
Start Time: 12:15 PM (15 Mins)
Speaker/Author: Jatin Jatin (Indian Institute of Science, India); M. Monish Murali (Indian Institute of Science Bangalore, India); Satendra Kumar Gautam and Mayank Shrivastava (Indian Institute of Science, India)
Presenter: Jatin Jatin

Abstract: In this work, for the first time, Drain-Extended vertically stacked Nanosheet-based HV device has been studied in the context of System-On-Chip (SoC) integration. Physical insights into the device performance and ESD reliability are elaborated using 3D TCAD process simulations. Finally, the performance and reliability co-design guidelines related to HV devices in Nanosheets technology have been discussed comprehensively.

62-5: Investigating Alternate Transport Mechanisms for novel ESD device development (Invited Talk)
Start Time: 12:30 PM (30 Mins)
Speaker/Author: Dr. Radhakrishnan Sithanandam, Micron Technology Inc
Presenter: Dr. Radhakrishnan Sithanandam

Abstract: Majority of the ESD devices using the CMOS technology uses with drift-diffusion transport mechanism or avalanche triggered bipolar action. This work explores the applicability of controlled impact ionization and band to band tunneling mechanisms for the ESD device development. Various testcases are evaluated through 3D-TCAD simulations, TLP and VFTLP measurements.

Session No: 63 | Session Title: Piezoelectric MEMS

Audi: 8 | 11:15 AM-12:45 PM | **Session Chair:** Prof. Dhiman Mallick
Track: MEMS/NEMS and Heterogeneously Integrated Devices (NEMS)
Date: 14-Dec-22

63-1: Design, Fabrication, Characterization & Modeling of a 1 GHz RF MEMS resonator for oscillator application (Invited Talk)
Start Time: 11:15 AM (30 Mins)
Speaker/Author: Prof. Deleep R. Nair, IIT Madras
Presenter: Prof. Deleep R. Nair

Abstract: The phenomenal accuracy and temperature stability of quartz oscillators has enabled it to rule the frequency control and timing devices market for around 100 years. It may sound ironic that despite quartz being a pure crystalline form of SiO2, it isn't compatible with the Silicon IC fabrication process. This prevents any possibility of on-chip integration and creates a bottleneck to the size reduction of electronic systems and circuit boards. One solution for this is to replace the quartz crystal with a MEMS based resonator which is CMOS process compatible. In this seminar, I will describe the design, fabrication, characterization and modeling of an RF MEMS resonator operating at around 1 GHz.

63-2: Mechanically Coupled Cantilever Beam Structure for Wideband Piezoelectric Energy Harvesting (Oral)
Start Time: 11:45 AM (15 Mins)
Speaker/Author: Nitika Batra and Bhaskar Mitra (IIT Delhi, India)
Presenter: Nitika Batra

Abstract: In this work, we report the mechanical coupling of the cantilever beams in a cascaded configuration employed using long and thin spring-like structures to increase the bandwidth for vibration energy harvesting. The outcomes of designing uni-beam, dual-beam, tri-beam, and quad-beam coupled energy harvesters are compared using COMSOL. Simulation results indicated that quad-beam coupled energy harvesters had a bandwidth of 8.9 Hz. Physical devices were fabricated and tested using PVDF-TrFE piezoelectric material.

63-3: Low Temperature and Dc Bias Dependence Study of Barium Strontium Titanate Based High Overtone Bulk Acoustic Resonator (HBAR) (Oral)
Start Time: 12:00 PM (15 Mins)
Speaker/Author: Kongbrailatpam Sandeep Sharma (CeNSE, IISC Bangalore, India); Jakkapally Pundareekam Goud (Yeungnam University, India); James Raju K c (University of Hyderabad & School of Physics, India); Gayatri Pillai (IISc Bangalore, India)
Presenter: Kongbrailatpam Sandeep Sharma

Abstract: This paper reports the study and characterization of a high overtone bulk acoustic resonator (HBAR) with varying dc bias voltages applied and with measurements performed at various temperature points. Important parameters of the resonators such as the effective coupling coefficient and quality factors are studied for the multiple resonant modes appearing in the frequency spectra with relation to effects from both temperature and dc bias applied. It is observed that the resonant modes intensity (S11, dB) and its distribution varies with different bias voltages as well as upon the polarity of the bias applied. Both the effective coupling coefficient and the quality factor (Q) of the modes are heavily influenced by the temperature at which the resonator operated. The transition temperature of the ferroelectric thin film Ba0.5Sr0.5TiO3 (BST) used as the transducer is also observed from the distribution of the coupling coefficient and quality factor with temperature. From the study of three different resonant modes (0.94 GHz, 1.52 GHz and 2.56 GHz), it is observed that the frequency quality factor product (fQ) has an inverse proportionality with temperature wherein with decrease in temperature, the recorded fQ increases. The dependence of fQ on temperature also increases with increase in frequency of the mode considered.

63-4: FSMA Based MEMS Magnetoelectric Sensor (Invited Talk)
Start Time: 12:15 PM (30 Mins)
Speaker/Author: Prof. Davinder Kaur Walia, Indian Institute Of Technology Roorkee
Presenter: Prof. Davinder Kaur Walia

Abstract: MEMS sensors based on magnetoelectric heterostructures have attracted great interest due to their capability to detect weak magnetic fields, showing high potential in applications like magnetic particle imaging. and biomagnetic field detection like magnetocardiography (MCG) and magnetoencephalography (MEG). These applications require sensor arrays with required resolution which can be achieved by MEMS technology. Among various magnetostrictive materials, ferromagnetic shape memory alloys (FSMAs) exhibit room temperature giant magnetostrictive effect and first-order martensite transformation. FSMAs have been used for magnetic actuation and magnetic field sensor applications. In this talk I will discuss about our current ongoing activities on Ferromagnetic shape memory materials which are combined with strong piezoelectrics in such a way that they can give rise to magnetoelectric composites, with interesting properties that are being applied in next generation four logic state memory devices, magnetic field sensing, biosensors and vibration damping device useful for MEMS applications.

Session No: 64 | Session Title: Machine Learning and Device Modelling

Audi: 9 | 11:15 AM-01:00 PM | **Session Chair:** Mr. Srikanth Srihari
Track: Modelling and Simulations (MS)
Date: 14-Dec-22

64-1: Machine Learning Techniques as Alternative to Physics Based Parametric Device Model Development (Invited Talk)
Start Time: 11:15 AM (30 Mins)
Speaker/Author: Dr. Sourajeet Roy, Indian Institute of Technology Roorkee, India
Presenter: Dr. Sourajeet Roy

Abstract: Continuous innovations in the field of semiconductor device architectures are ongoing to meet the growing demands of higher performance, smaller power budgets, and higher frequency of device operation at smaller form factors. Therefore, electronic design automation (EDA) tools have become essential for the timely simulation and analysis of these devices. Current EDA tools entail the solution of the physics partial differential equations related to the electrostatics and charge transport of semiconductor devices using traditional finite-

element/finite-difference methods, as in TCAD. Such simulators are extremely time and memory hungry, especially when probing the performance of the device across massively large parameter spaces. In this talk, I will highlight the opportunities presented by emerging machine learning (ML) techniques as extremely efficient alternatives to the standard rigorous physics-based approach for semiconductor devices. Specifically, my talk will focus on the new concept of prior knowledge-based machine learning as a way to enhance the learning ability and trainability of modern ML techniques.

64-2: An Efficient Variability-Aware Control Variate-Assisted Neural Network Model for Advanced Nanoscale Transistors (Oral)
Start Time: 11:45 AM (15 Mins)
Speaker/Author: Srishti Parandiyal, Anamika Singh, Kumar Sheelvardhan, Surila Guglani and M Ehteshamuddin (Indian Institute of Technology Roorkee, India); Sourajeet Roy and Avirup Dasgupta (IIT Roorkee, India)
Presenter: Srishti Parandiyal

Abstract: In this paper, a novel artificial neural network (ANN) has been developed for the efficient variation-aware modeling of current-voltage (I-V) characteristics of general nanoscale devices. The key innovation of this work lies in the development of a new control variate strategy to significantly shrink the number of technology computer-aided design (TCAD) device simulations required to train the ANN model. Consequently, the proposed ANN model can emulate the drain current of the target device as analytic functions of the device geometry, material, and bias voltages at much smaller computational costs than conventional ANN models. A validation example of a 14nm fin field effect transistor (FinFET) is provided in this paper.

64-3: AI/ML Based 100X Faster Thermal Analysis Methodology With 5% Accuracy (Oral)
Start Time: 12:00 PM (15 Mins)
Speaker/Author: Saravanakumar Mahalingam (Thermal Analyst & Intel India, India)
Presenter: Saravanakumar Mahalingam

Abstract: The new generation SOCs requires a thermal solution to maintain temperatures within operating limits. Design and optimization of suitable thermal solution and upfront thermal analysis are key to design thermal friendly design based on all critical workloads in very fast manner.
There are two common methods of predicting SOC thermal performance: computational simulation and experimental measurement. These two methods involve complicated operations and experimental setup. Therefore, it is quite difficult to build computational simulations that fully capture the complicated logical relationships between the properties of a material, geometry, power and their related factors, and some of these relationships may even be unknown. Therefore, there is an urgent need to develop intelligent and high-performance prediction models that can correctly predict the SOC thermal solution at a low temporal and computational cost. In this work, a new methodology for optimization of SOC Thermal Performance process is developed, using Regression-Based Reduced-Order Modelling Techniques. This methodology can be applied to any type of platform configurations to reduce computation effort, results reduction in overall design time and cost. Also, this approach (Implemented through software applications-tool) can be deployed internally as well as customer experience thermal tool, allows customers to predict the optimum thermal solutions tailored to their project requirements. This tool is developed using blending different regression models for better prediction of SOC thermal performance, it comprises different types of heat sink models (extruded, folded fin, heat pipe embedded, and vapor chamber) allows user to select right tradeoff between performance and cost. In this work, a new methodology to estimate thermal performance analysis is demonstrated for complex inhouse SOC with about 100X faster and with about 95% accurate reference to industry solutions available. In this analysis all data are normalized to ensure sensitive design details are protected.

64-4: Design for Robust and Efficient Neuromorphic Photonic Accelerator (Oral)
Start Time: 12:15 PM (15 Mins)
Speaker/Author: Samarth Aggarwal, Bowei Dong, June Sang Lee and Mengyun Wang (University of Oxford, United Kingdom (Great Britain)); Andrew Katumba (Gent University & IMEC, Belgium); Peter Bienstman (Gent University - imec, Belgium); Harish Bhaskaran (Oxford University, United Kingdom (Great Britain))
Presenter: Samarth Aggarwal

Abstract: In this work, we propose a novel architecture for building a robust integrated photonic neuromorphic accelerator based on a crossbar array design. Our architecture is based on an asymmetric multimode Y-coupler. A Y-coupler has the inherent benefit of high fabrication tolerance and broad optical bandwidth. From simulations, we show that our proposed Y-coupler has high coupling efficiency. Using modal decomposition analysis of our

coupler, we numerically estimate the energy efficiency performance of a large-scale photonic network and show a 10% improvement in energy efficiency for large-scale photonic networks with high fabrication tolerance and broadband application and a small footprint.

64-5: Co-design from processes to circuits and application of machine-learning for device-variability prediction (Invited Talk)
Start Time: 12:30 PM (30 Mins)
Speaker/Author: Dr. Sushant Mittal, Lam Research, India
Presenter: Dr. Sushant Mittal

Abstract: In this talk, we will discuss how can we co-design semiconductor processes, devices, and circuits, with the help of couple of case studies. Benefits of such co-design at a cutting-edge node will also be discussed. In the next part, machine-learning based device variability prediction framework will be discussed.

Session No: 65 | Session Title: Advances in Power Electronics Circuits
Audi: 10 | 11:15 AM-01:00 PM | **Session Chair:** Dr. Sukhendu Deb Roy
Track: Advanced Power Device Technology (APDT)
Date: 14-Dec-22

65-1: Advanced Power Processor for Digital Infrastructure (Invited Talk)
Start Time: 11:15 AM (30 Mins)
Speaker/Author: Dr. Harshad Mehta, Silicon Power Corp, USA
Presenter: Dr. Harshad Mehta

Abstract: The members of scientific and technical communities in power semiconductor device technology are very much familiar with MOSFETS, IGBTs, SCRs, and GTOs.However, most of the users of these products view these acronyms as alphabet soup. We must conceive “the power processor,” a useful black box that provide the most optimum solution for given input and ideal desired output using the best power semiconductor device that provides the ultimate flexibility, lowest losses, highest switching speed controllable with firmware and software. All of these attributes can be summarized as an “Ideal Switch”. This paper will summarize and provide an overview of such “Ideal Switch” configurations as AC Power Processor and DC Power Processor integrating common Alphabet Soup devices offering most advanced optimum high power building block that can leverage a wide spectrum of applications with super economic benefits for modern digital infrastructure.

65-2: Silicon Device Based Power Electronic Converters – Applications and Research in Power Electronics (Invited Talk)
Start Time: 11:45 AM (30 Mins)
Speaker/Author: Dr. Arunkumar G, Vellore Institute of Technology (VIT), Vellore, Tamil nadu, India
Presenter: Dr. Arunkumar G

Abstract: Silicon devices have been in use for a long time for power applications. MOSFETS, IGBTs, SJ MOSFETS, GTOs and other devices have been used in power converters for applications such as Electric Vehicle (EV) battery charging, wireless charging, DC gird, renewable – fed converters, etc. The expertise of our team is in hardware implementation of these converter topologies. Various non-isolated and isolated converters have been tested and validated with for these applications and for simultaneous charging of multiple Li – ion batteries of different ratings, CLLC converter for charging of multiple batteries, patented wireless charging of 48 V battery from a 36 V source etc. A discussion of the implementation of these projects with practical tips for researchers will be a major taking point of the talk.

65-3: Device-Circuit Co-Design and ESD/HCI Reliability Aware Design of Field Plated RF LDMOS Devices (Oral)
Start Time: 12:15 PM (15 Mins)
Speaker/Author: Harsha B Variar (Indian Institute of Science, India); Ajay Singh (Indian Institute of Science Bangalore, India); Jhnanesh Somayaji (Srinivasnagar, India); Mayank Shrivastava (Indian Institute of Science Bangalore, India)
Presenter: Harsha B Variar

Abstract: This work explores the scope of Laterally Double Diffused Metal Oxide Semiconductor (LDMOS) for high off-state breakdown voltage with significantly low on-resistance and which can deliver output power above

1000W to the load for the frequency range 27MHz to 3.6GHz. Optimization of field plates (gate field plate and drain field plate) has been done to achieve high breakdown voltage.
Further optimization has been done by keeping floating the substrate contact and without sinker of RF LDMOS to achieve more off-state breakdown voltage. The optimization offers 120V off-state breakdown voltage. A model card was generated by using HiSim compact model in IC-CAP industry simulation software to investigate the radio frequency power amplifier performance
of FP RF LDMOS designs. The RFPA performance of FP RF LDMOS designs was investigated on Advance Design System simulation software which offered drain efficiency (ηD) of 87%, output power(Pout) more than 60dBm and 25 dBm Gain at 1dB compression point compared to the commercially available NXP device (MRFE6VP61K25H). Electrostatic Discharge (ESD) robustness was studied for
the FP RF LDMOS designs as ESD has been identified as a source of damage to unprotected devices. Hot Carrier Injection (HCI) reliability was also investigated to address the complete reliability of these devices.

65-4: Dual Active Bridge: Closed Form Equations for Voltage Fed and Current Fed Converters with Soft Switching Criteria. (Invited Talk)
Start Time: 12:30 PM (30 Mins)
Speaker/Author: Mr. Archit Asthana, Chara Technology
Presenter: Mr. Archit Asthana

Abstract: Dual Active Bridge is becoming popular day by day because of the high power handling capability, ease in achieving soft-switching, simpler operation, etc. It is a core interfacing component in High Frequency Links power conversion systems for bidirectional power such as in solid state transformer (SST) etc. Isolation through high frequency transformer sometimes also aid in achieving a more efficient solution by proper choice of turns ratio. Here analysis has been carried out for an application which has a moderately high turns ratio. The focus was to arrive at a design methodology which yield minimum loss. For this probable topology candidates was studied and a comparative analysis was made. This design methodology can also be extended and tailor made for any specification. This talk revolves around the design of a DAB Converter for minimum loss. Two types of DAB- Voltage-Fed and Current-Fed, have been studied extensively and then the design of the topology is shown with comparison.

Session No: 66 | Session Title: Intelligent Memories
Audi: 11 | 11:15 AM-01:15 PM | **Session Chair:** Prof Udayan Ganguly
Track: Advanced Memory Technologies (AMT)
Date: 14-Dec-22

66-1: Neural network accelerators with emerging memory devices: status and challenges (Invited Talk)
Start Time: 11:15 AM (30 Mins)
Speaker/Author: Prof. Daniele Ielmini, Politecnico di Milano
Presenter: Prof. Daniele Ielmini

Abstract: In-memory computing (IMC) has emerged as one of the most promising concepts to improve the energy efficiency and throughput of deep neural networks. At the same time, there are several key challenges of adopting emerging memories for IMC, including feasibility, reliability and maturity. This talk will address the status and challenges of IMC from a device perspective. State-of-the-art emerging memories will be compared in terms of conductance and its variation, which play a key role in the inference accuracy and scalability of IMC. A quantitative benchmark will be proposed by assessing throughput, area and energy efficiency for various memory technologies.

66-2: Recent Advances in the Understanding of Random Telegraph Noise in 3-D NAND Flash memories (Invited Paper)
Start Time: 11:45 AM (30 Mins)
Speaker/Author: Gerardo Malavena, Mattia Giulianini and Christian Monzio Compagnoni (Politecnico di Milano, Italy); Luca Chiavarone (Micron Technology Inc., Italy); Alessandro Spinelli (Politecnico di Milano, Italy)
Presenter: Gerardo Malavena

Abstract: The transition from planar (2D) to three-dimensional (3D) arrays represented a turning point for the phenomenology of random telegraph noise (RTN) in NAND Flash technologies. The relevant changes in the cell structure and in the process integration at the basis of that transition, in fact,

strongly impacted some major aspects of the physics responsible for RTN and for its dependence on the array working conditions. In this paper, we comprehensively discuss the recent advances in the exploration and in the understanding of such physics in 3D arrays. The discussion allows us to identify the most relevant details related to array operation, which must be addressed to mitigate the reliability issues arising from RTN, contributing to the attempt to prolong the successful evolutionary trends of 3D NAND Flash technologies.

66-3: Mimicking Synaptic Behaviors With Junctionless Transistor for Low Power Neuromorphic Computing (Oral)
Start Time: 12:15 PM (15 Mins)
Speaker/Author: Md. Hasan Raza Ansari (King Abdullah University of Science and Technology (KAUST) & NA, Saudi Arabia); Hanrui Li and Nazek El-Atab (King Abdullah University of Science and Technology, Saudi Arabia)
Presenter: Md. Hasan Raza Ansari

Abstract: This work highlights the application of a junctionless (JL) transistor with charge trapping mechanism as an artificial synaptic device for neuromorphic computing. In this work, synapse behaviors ((short-term potentiation (STP), long-term potentiation (LTP), and depression (LTD))) have been validated and analyzed by storing the positive charges (holes) in the floating body and charge trapping nitride layer. JL device can be operated at a lower drain voltage (VDS = 0.8 V) to trigger the band-to-band tunneling and impact ionization mechanisms. The device achieves a higher and linear conductance value, and the non-linearity value for LTP is 0.1, which is beneficial for neural networks. Estimated conductance values from the device are utilized to estimate the pattern recognition and achieve an accuracy of ~ 85 % with the CNN algorithm and CIFAR-10 datasets.

66-4: Memristive Switching in Cu2O1-x/CuO1-y Heterojunction Due to Vacancies (Oral)
Start Time: 12:30 PM (15 Mins)
Speaker/Author: Vivek Singh (Centre of Nanoscience and Engineering, IISc Bangalore, India); Jyoti Sinha (KU Leuven, Belgium & IMEC Belgium, Belgium); Sushobhan Avasthi (Indian Institute of Science & Centre for Nano Science and Engineering (CeNSE), India)
Presenter: Vivek Singh

Abstract: The migration of copper vacancies across the heterojunction interface is suggested as a possible explanation for the device's observed resistive switching characteristic. Overall, memristor properties that exhibit good consistency in dependability data like repeatability, endurance, and retention yield the best results.

66-5: Phase Change Memory Technology for High Speed Computing (Invited Talk)
Start Time: 12:45 PM (30 Mins)
Speaker/Author: Prof. Anbarasu Manivannan, Indian Institute of Technology Madras, India
Presenter: Prof. Anbarasu Manivannan

Abstract: In the realm of next generation computing, chalcogenide based Phase Change Memory (PCM) offers promising features for a 'universal memory' owing to all-round characteristics including high-speed and non-volatility. However, realizing an ultrafast switching is still a key challenge for faster programming. This talk will present exhaustive experimental results on electrical switching of Ge-Sb-Te, Ag, In-doped Sb2Te and In-Sb-Te based PCM devices including ultrafast electrical switching dynamics, voltage-dependent transient characteristics in picosecond timescale using a custom-built advanced programmable electrical test setup. Furthermore, a trajectory map for defining the ultimate speed of PCM devices will be discussed on the basis of field-dependent transient dynamics in picosecond timescale for enabling the ultimate speed of PCM devices would pave a way towards realizing 'universal memory' for future computing.

Session No: 67 | Session Title: Applications of 2D materials and devices 2

Audi: 1 | 02:30 PM-04:15 PM | **Session Chair:** Prof. Bent Weber
Track: 2D Material Based Technologies (2DT)
Date: 14-Dec-22

67-1: Transition Metal Dichalcogenides based Heterostructures for Ultra-sensitive Environmental Gas Sensors (Invited Talk)
Start Time: 02:30 PM (30 Mins)
Speaker/Author: Dr. Branson Belle, SINTEF, Norway
Presenter: Dr. Branson Belle

Abstract: The isolation of graphene has heralded a new class of material research in 2D materials. Due to their high mobilities, tuneable bandgaps and surface to volume ratios, 2D materials have shown promising performance as gas sensors. Moreover, heterostructures can further enhance sensitivity and other device properties. Details of heterostructure gas sensor assembly and adhesion between 2D materials will be discussed. Additionally, the performance of these gas sensors and their sensing mechanism will be presented.

67-2: Inkjet-Printed WS2 and MoSe2 Transistors With Edge-FET Architecture and Near-Vertical Electronic Transport (Oral)
Start Time: 03:00 PM (15 Mins)
Speaker/Author: Sandeep Kumar Mondal (Indian Institute of Science, India); Subho Dasgupta (Indian Institute of Science (IISc), Bangalore, India)
Presenter: Sandeep Kumar Mondal

Abstract: Two dimensional (2D) semiconductors combine the advantages of both oxide and organic semiconductor world, namely, high carrier mobility, environmental stability, as well as room temperature processability, flexibility and the availability of both high carrier mobility n- and p-type semiconductor variants. However, for their realization in flexible, wearable electronics, high throughput solution processing techniques, such as printing is essential. However, when solution-processed, the performance of the devices deteriorates substantially due to huge inter-flake resistance. To overcome this challenge, here we propose and demonstrate an unconventional thin film transistor (TFT) device architecture which can circumvent the shortcoming of large inter-flake resistance by transforming the TFTs into predominantly intraflake transport edge-FETs. Using this edge-FET device architecture, here we present TFTs printed from chemically exfoliated WS2 and MoSe2 inks, with 106 μA/μm and 25 μA/μm width-normalized, On-state current density, respectively. On the other hand, the maximum On-Off ratio observed in these printed TFTs have also been large, as high as 10 7 has been recorded, which is surely a rarity in solution-processed 2D electronics. In addition, a tunable channel capacitance mediated subthermionic transport with minimum subthreshold slope of 36 mV/dec has also been observed.

67-3: Unveiling Additional Ambient Degradation Issues of Phosphorene FETs Under Laser Exposure and Positive Gate Bias (Oral)
Start Time: 03:15 PM (15 Mins)
Speaker/Author: Jeevesh Kumar and Utpreksh Patbhaje (Indian Institute of Science, India); Mayank Shrivastava (Indian Institute of Science Bangalore, India)
Presenter: Jeevesh Kumar

Abstract: Despite many extraordinary properties, phosphorene is not favorable for device applications due to its gradual degradation in ambient environmental conditions. The degradation process is mainly initiated by oxygen molecules attacking the lone pair of phosphorus atoms. However, the same is assisted by additional factors like water molecules, phosphorus vacancy, and negative gate bias. This work extended the journey further and revealed the role of positive gate bias and laser exposure on phosphorene degradation in the ambient environment. The work shows that in the case of phosphorene-based Field Effect Transistors (FETs), the material's degradation due to oxygen molecules can also be influenced by excess electrons due to positive gate bias in the channel. The first-principles molecular dynamics (MD) computations and Raman characterizations show that phosphorene degrades faster under positive gate bias (excess electron) than in pristine conditions (unbiased). The rapid degradation is mainly due to the enhanced oxidation by the excess electrons in the channel. The computational findings are experimentally verified using Raman characterization over phosphorene FETs. Additionally, the work also discusses the role of laser light on phosphorene degradation. The laser light does not play a direct role in pristine phosphorene degradation. However, the same assists the degradation process by etching the residual oxide formed over the phosphorene surface due to its ambient degradation. Our study reveals a unique reliability issue related to phosphorene FETs that gives a broader picture of the limitation of the material in the technology applications.

67-4: A Monolithic Stochastic Computing Architecture for Energy Efficient Arithmetic (Oral)
Start Time: 03:30 PM (15 Mins)
Speaker/Author: Harikrishnan Ravichandran, Yikai Zheng, Thomas F Schranghamer, Nicholas Trainor and Joan M Redwing (The Pennsylvania State University, USA); Saptarshi Das (Pennsylvania State University, USA)
Presenter: Harikrishnan Ravichandran

Abstract: A change in paradigm that can trade precision for energy and resource efficiency has been sought for many computing applications in the energy- and the hardware-intensive era of artificial intelligence (AI). The ongoing revolution in AI, championed by the aggressive downscaling of feature sizes in CMOS technology has

enabled the implementation of deep learning and other sophisticated machine learning algorithms. However, there is a significant infrastructure cost associated with advanced AI and computing systems. The von Neumann architecture necessitates frequent data shuttling between the arithmetic and the memory units to run algorithms that require arithmetic operations that are executed using logic circuits. These circuits consist of hundreds of transistors that occupy a large area and consume a significant amount of energy. Stochastic computing (SC) is an attractive alternative where arithmetic operations can be performed using simple logic gates yielding energy and area efficiency. A single AND gate can perform multiplication while the same operation is carried out using high transistor count full adder circuits in CMOS architecture. Similarly, stochastic addition and subtraction can be performed using a multiplexer (MUX) and XOR gates, respectively. SC is highly error-tolerant and is also rooted in bio-inspired computing since the brain can process information in the presence of noise and can learn, adapt, and make the right decision at the cost of miniscule energy expenditure. While it is possible to accelerate SC using traditional silicon complementary metal oxide semiconductor (CMOS) technology and emerging technologies like memristors and spin-based devices, the need for extensive hardware investment to generate stochastic bits (s-bit), the fundamental computing primitive for SC, makes it less attractive. Here, we overcome the above-mentioned limitations by introducing a standalone SC architecture embedded in memory, which is based on two-dimensional (2D) memtransistors. Our main contributions are 1) the realization of an area and energy-efficient six-transistor (6T) s-bit generator circuit that exploits the inherent stochasticity in the carrier trapping and detrapping phenomena in the gate insulator of the 2D memtransistors and combines it with an inverting amplifier and a programmable thresholding inverter to obtain s-bits and 2) integration of s-bit generators with 2D memtransistor based logic gates such as AND, MUX, XOR, and OR gates to demonstrate arithmetic operations such as multiplication, addition, and subtraction. Our SC architecture consumes a miniscule amount of energy < 1 nanojoules for s-bit generation and to perform arithmetic operations.

67-5: A Synergistic Hardware Neural Network With Enhanced Learning and Accurate Inference Enabled by Programmable and Complementary 2D FETs (Oral)
Start Time: 03:45 PM (15 Mins)
Speaker/Author: Rahul Pendurthi (Pennsylvannia State University, USA); Darsith Jayachandran and Saptarshi Das (Pennsylvania State University, USA)
Presenter: Rahul Pendurthi

Abstract: Recently, unsupervised and reinforcement learning in ANNs have shown remarkable results in defeating professional players in the game of Go, one of the most challenging for artificial intelligence (AI). While software ANNs can leverage sophisticated supervised learning algorithms, their hardware implementation remains challenging and resource extensive. Here we introduce a novel synergistic hardware neural network (SHNN) that allows semi-unsupervised learning and inference by exploiting complementary transport in n-type monolayer MoS 2 and p-type vanadium (V) doped bilayer WSe 2 field effect transistors (FETs) integrated with an analog, non-volatile, and programmable memory.

67-6: A Secure Random Key Generator Based on Integrated Circuits Enabled by Atomically Thin Two-Dimensional Materials (Oral)
Start Time: 04:00 PM (15 Mins)
Speaker/Author: Harikrishnan Ravichandran (The Pennsylvania State University, USA); Dipanjan Sen, Akshay Wali and Saptarshi Das (Pennsylvania State University, USA)
Presenter: Harikrishnan Ravichandran

Abstract: Information exchange is the foundational backbone of all modern-day communication technology such as Internet of Things (IoT) which involves humongous volumes of data shuttling. To guarantee the security of encryption and decryption schemes for exchanging such information, generation of high-quality true random numbers (TRNG) are critical. In this letter, we have proposed a three-stage inverter (TSI) based true random number generator (TRNG) based on large area grown monolayer MoS2 field effect transistors (FET), which offer random stochasticity due to the charge trapping and de-trapping in the Al2O3/HfO2/Al2O3 gate dielectric stack. Our TRNG offers high entropy, uniformity, and a decent hamming distance. Moreover, the NIST randomness tests ensure that the key is unique and truly random in nature.

Session No: 68 | Session Title: Next-Generation of Commercial Solar Technologies
Audi: 2 | 02:30 PM-04:15 PM | **Session Chair:** Prof. Dinesh Kabra
Track: Solar Cells & Photodetectors: Physics, Device, & Modules (SP)
Date: 14-Dec-22

68-1: Status report on silicon heterojunction solar cell and related PV technologies (Invited Talk)
Start Time: 02:30 PM (30 Mins)
Speaker/Author: Dr. Kaining Ding, Forschungszentrum Jülich GmbH
Presenter: Dr. Kaining Ding

Abstract: The talk aims at giving an introduction and an overview on silicon heterojunction (SHJ) solar cell technology as a next-generation mainstream PV mass product. Firstly, the device concept together with a historical review will be introduced. Then, a report on the current status of this technology from research, industry and supply chain point of view should reveal the potential and challenge of this technology in the near future. In addition, this contribution will adress the perovskite--SHJ-tandem solar cell as a technology to overcome the 30% efficiency threshold.

68-2: Enhanced Photoresponse of SnS2/Si Nanowire Heterostructure by KOH Etching (Oral)
Start Time: 03:00 PM (15 Mins)
Speaker/Author: Sourav Das, Sourabh Pal, Debabrata Mandal, Pallab Banerji, Amreesh Chandra and Rabaya Basori (Indian Institute of Technology Kharagpur, India)
Presenter: Rabaya Basori

Abstract: Nanowire (NW) heterostructures offer a new platform for photodetection applications. Improvement of NW heterostructure device performance for photodetector application is a challenging field of research. Herein, we report an increased photoresponsive performance of SnS2/SiNWs simply by etching the SiNWs surface in KOH. SnS2 nanocomposites are spin coated on the surface of without-etched and with-etched (1 minute) SiNWs to make the heterostructure, and measured the optoelectronic characteristics. A comparison of optical and electronic properties of SnS2/SiNWs (with and without etched) is presented, with emphasis on the effect of KOH etching on device performance improvement.

68-3: Large-Area Back Contact Electrodes for Perovskite Solar Cells Using Nanosphere Lithographic Techniques (Oral)
Start Time: 03:15 PM (15 Mins)
Speaker/Author: Poulomi Chakrabarty (CeNSE, IISC, India); Poyoja Rout (IISC, India); Laxman Gouda and Aditya Sadhanala (Indian Institute of Science, India)
Presenter: Poulomi Chakrabarty

Abstract: Hybrid metal-halide perovskite solar cells (PSC), developed on a lab scale, have been shown to exhibit high power conversion efficiency (PCE). Hence, developing these devices on an industrial scale is being pursued. Compared to planar devices, back-contact interdigitated electrode (BCIE) architectures have several potential benefits: low reflection and parasitic absorption in metal contacts, a large active area for light absorption, and higher PCE. In this paper, we have successfully fabricated large-area (~ 2.25 cm2) nanopatterned ITO/TiO2/SiO2/Ni electrodes of feature size ~ 350 nm using a self-assembled colloidal monolayer as a sacrificial template. The novelty of the design lies in the fact that the resolution of electrode spacing (350 nm) is one order lower than that of state-of-the-art BCIEs, making it comparable to the perovskite material's average diffusion length and thereby improving the PCE of the PSC. This kind of nanosphere-lithography-mediated fabrication of honeycomb back-contact electrodes with 100% device active area will lead to new opportunities related to large area low-cost back-contact perovskite solar cells.

68-4: Performance Enhancement by Introducing Different Chlorinated Salts in the SnO2 Electron Transfer Layer of Perovskite Solar Cells (Oral)
Start Time: 03:30 PM (15 Mins)
Speaker/Author: Apoorva Singh (Indian Institute of Science Bengaluru, India); Bidisha Nath, Ashutosh P and Praveen C Ramamurthy (Indian Institute of Science, India)
Presenter: Apoorva Singh

Abstract: Tin oxide (SnO2) is one of the important and commonly used electron transfer layers (ETLs) in the planar structure of perovskite solar cells (PSCs). Doping the SnO2 layer with chlorinated salts such as potassium

chloride (KCl) has been reported to improve the power conversion efficiency (PCE), intriguing further exploration of other chlorinated salts. Herein, the results from various chlorinated salts in addition to KCl are evaluated. It was observed, that though the PSCs with KCl doped SnO2 layer yield the best PCE (~17%), the ETL layer doped with other chlorinated salts such as sodium chloride (NaCl) and Iron chloride (FeCl3) also showed improvement in performance from the pristine SnO2 (~15 %). Moreover, the results from the SnO2-NaCl-based devices are found to be comparable to the SnO2-KCl. Performance enhancement is attributed to the passivation of defects in the interface and reduction in the non-radiative recombination losses. The established trend is supported by the current-voltage (J-V) and photoluminescence (PL) studies.

68-5: Advanced Characterization of Silicon Solar Cells and Materials (Invited Talk)
Start Time: 03:45 PM (30 Mins)
Speaker/Author: Dr. Ron Sinton, Sinton Instruments, USA
Presenter: Dr. Ron Sinton

Abstract: The electronic quality of silicon material and wafer bulk and surface recombination can be tracked through the entire value chain during ingot to solar cell to module manufacture. This talk will describe the use of excess-carrier-lifetime measurements throughout the process. In addition to applying this technique for process optimization and control, the use of lifetime measurements to study the various degradation mechanisms under light and temperature stress for high-efficiency solar cells will be described. This will include eddy-current lifetime-measurement techniques as well as the interpretation of current-voltage and additional data at the cell, module, and array tests.

Session No: 69 | Session Title: GaN and SiC Device Technology & Physics - 2

Audi: 3 | 02:30 PM-04:15 PM | **Session Chair:** Dr. Ritu Sodhi
Track: Wide Bandgap Power Semiconductor Technologies (WPSD)
Date: 14-Dec-22

69-1: Progress in Growth and Fabrication of AlGaN LEDs on SiC Substrates (Invited Talk)
Start Time: 02:30 PM (30 Mins)
Speaker/Author: Prof. Siddharth Rajan, The Ohio State University
Presenter: Prof. Siddharth Rajan

Abstract: The disinfection industry would greatly benefit from efficient high-power deep-ultraviolet light-emitting diodes (UV-C LEDs). In this talk, I discuss progress in the growth and fabrication of AlGaN LEDs on SiC Substrates. First, we will discuss the physics of lighting with double heterostructures LEDs and the physics of nitride semiconductors. Then I will discuss the development of epitaxial growth and processing techniques for the best demonstration of UV LEDs (260—275 nm) on SiC substrate, which was enabled by novel thin-film flip-chip processes and resulted in high LED light extraction efficiency relative to planner sapphire or AlN substrates. Moreover, I will discuss tunnel junction UV LEDs and how they can significantly improve LED performance and the potential of UV disinfection.

69-2: Modeling and Design of Superjunctions in Silicon Carbide (Invited Talk)
Start Time: 03:00 PM (30 Mins)
Speaker/Author: Prof. Shreepad Karmalkar, IIT Bhubaneswar (at the time of presentation)
Presenter: Prof. Shreepad Karmalkar

Abstract: Superjunctions yield a lower specific on-resistance, RONSP, for a given breakdown voltage, than conventional p-n junctions. We derive (a) a new theoretical lower limit of RONSP for an ideal balanced superjunction that is 30 % lower than prior works, (b) closed-form design equations for a practical superjunction considering process variations for the first time, and show that the optimum p-pillar aspect ratio is < 15 whereas prior works have tried raising this ratio beyond 25. We also propose charge sheet superjunction as a viable alternative to superjunction in SiC material to avoid complexities associated with fabrication of p-pillars in SiC.

69-3: Hot Electron Interaction With C-Doped GaN Buffer and Resultant Gate Leakage Degradation in AlGaN/GaN HEMTs (Oral)
Start Time: 03:30 PM (15 Mins)
Speaker/Author: Rajarshi Roy Chaudhuri, Vipin Joshi and Sayak Dutta Gupta (Indian Institute of Science, India); Mayank Shrivastava (Indian Institute of Science Bangalore, India)
Presenter: Rajarshi Roy Chaudhuri

Abstract: This work reports semi-ON state DC stress induced gate degradation in AlGaN/GaN HEMTs on C-doped GaN buffer. A channel electric field and hot electron energy dependent critical drain stress voltage was found to govern the degradation. A mechanism based on hot electron-buffer trap interaction induced thermos-elastic stress build-up and subsequent defect formation in GaN buffer is proposed.

69-4: Trapping effects in High-Power 4H-Silicon Carbide (4H-SiC) Bipolar PiN Rectifiers (Invited Talk)
Start Time: 03:45 PM (30 Mins)
Speaker/Author: Dr. P. Vigneshwara Raja, IIT Dharwad
Presenter: Dr. P. Vigneshwara Raja

Abstract: Silicon carbide (4H-SiC) PiN diodes demonstrated ultra-high breakdown voltage (VBR < -10 kV) and extremely low reverse leakage current. The PiN rectifiers benefit from the drift conductivity modulation due to the minority carrier injection process, which mitigates the high-resistance of the voltage blocking layer. Nevertheless, performance limiting defects (Z1/2 and EH6/7) commonly exist in the drift layer. Additional trap levels are created in the epilayer during the Al-ion-implantation process. These traps restrict the maximum achievable performance of the PiN diodes.
The talk describes the identification of electrically active traps in the PiN diodes by Deep Level Transient Fourier Spectroscopy (DLTFS). The charge trapping induced changes in the current handling capability, on-resistance, leakage current and breakdown voltage of the PiN rectifiers are presented.

Session No: 70 | Session Title: Advanced Logic Devices

Audi: 4 | 02:30 PM-04:15 PM | **Session Chair:** Dr. Julien Ryckaert
Track: Advanced Logic Technologies (ALT)
Date: 14-Dec-22

70-1: Towards extreme scaling of CMOS technology using Forksheet and CFET (Invited Talk)
Start Time: 02:30 PM (30 Mins)
Speaker/Author: Dr. Pieter Weckx, Imec Belgium
Presenter: Dr. Pieter Weckx

Abstract: Scaling below 3nm will bring us far into the post FinFET era where extremely scaled logic standard cell heights and SRAM will limit the nanosheet scalability. The novel forksheet device architecture has been proposed as an ultimate scaling device towards 2nm and beyond. Furthermore, complementary FETs (CFETs) offer promise of ultimate scaling beyond the 1nm node and the ability to integrate alternate high mobility channels. Beyond CFETs, 2D materials such as MoS2, WS2 or HfS2 can be used to form atomic channel transistors, offering high mobilities and gate length scaling potential.

70-2: Nanosheet GAA Transistors (NsFETs) for High Performance Computing (Invited Talk)
Start Time: 03:00 PM (30 Mins)
Speaker/Author: Prof. Nihar Ranjan Mohapatra, Indian Institute of Technology Gandhinagar
Presenter: Prof. Nihar Ranjan Mohapatra

Abstract: Recent CMOS device scaling is driven by track height scaling to compensate slowdown in pitch scaling. The 5nm CMOS node uses 6 track standard cell with 2 fins/device. To sustain track height scaling, the fins/device need to be reduced to 1, which causes drastic drive current degradation. To overcome drive current degradation, the nanosheet architecture is adopted for 3nm CMOS node and beyond. The NsFETs provide wider effective channel width/footprint and better gate electrostatics than FinFETs. Further, the NsFETs have Quantum Mechanical Confinement (QMC) of charge carriers. The QMC alters the density of states (DOS), inversion charge density, threshold voltage and mobility of carriers. Several material innovations like, (a) Si, SiGe channel, (b) process induced strain management and (c) Si capped Ge channel are currently being pursued by industries and academia. This talk will discuss the material and structural innovations in NsFETs needed for high performance computing.

70-3: Device Design Aware and Interface Thermal Resistance Assisted Self-Heating Analysis in Nanosheet FET (Oral)
Start Time: 03:30 PM (15 Mins)
Speaker/Author: Sunil Rathore (PDPM-IIITDM & IEEE Member, India); Rajeewa Kumar Jaisawal (PDPM IIITDM Jabalpur, India); Pravin Kondekar (PDPM IIITDM Jabalpur, Madhya Pradesh, India); Shashank Kumar

Banchhor (Indian Institute of Technology Roorkee, India); Ankit Dixit and Navjeet Bagga (PDPM IIITDM Jabalpur, India)
Presenter: Sunil Rathore

Abstract: The nanoscaled geometrical confinement of the Nanosheet FET (NSHFET) has severely aggravated the self-heating effect, affecting the device's characteristics, such as lattice temperature, thermal contact resistance, and drive current. In this paper, we investigated the self-heating effect (SHE) in the NSHFET using well-calibrated TCAD models. We analyzed (i) the behavior of spatial device lattice temperature (TD) gradient in a gate-all-around (GAA) NSHFET; (ii) the impact of varying the drain, source, and gate electrode thermal contact resistances (Rth DSG). (iii) a fair comparison of electrical and thermal characteristics of SOI FinFET, bulk FinFET, and NSHFET based on the percentage change in subthreshold slope (SS), drain-induced barrier lowering (DIBL), drain current, etc. Further, we proposed the design guideline to mitigate SHE-induced thermal degradation in Nanosheet FET.

70-4: Engineering CFETs for A5 nodes and beyond (Invited Talk)
Start Time: 03:45 PM (30 Mins)
Speaker/Author: Dr. Sujith Subramanian, imec, Belgium
Presenter: Dr. Sujith Subramanian

Abstract: Complementary FET (CFET) is a promising candidate to push CMOS scaling beyond nanosheets and forksheets. CFET is formed by stacking an NMOS and PMOS device on top of each other. Area scaling is achieved by moving the N/P separation from the horizontal plane to the vertical plane. Fabrication of a CFET introduces significant integration challenges as we move away from the conventional processes used for CMOS devices. In this talk, we discuss how to fabricate a CFET (monolithic and sequential), the integration challenges that come with it, and potential areas where innovations are needed to enable this complex device architecture.

Session No: 71 | Session Title: Flexible and Smart Systems for Digital World

Audi: 5 | 02:30 PM-03:45 PM | **Session Chair:** Prof. Shree Prakash Tiwari
Track: Macroelectronics & Displays: Devices, Circuits & Systems (DIS)
Date: 14-Dec-22

71-1: In-Memory Sensing for the Digital Transformation (Invited Talk)
Start Time: 02:30 PM (30 Mins)
Speaker/Author: Prof. Nazek El-Atab, King Abdullah University of Science and Technology
Presenter: Prof. Nazek El-Atab

Abstract:
Since its emergence, Internet-of-Things (IoT) has brought numerous benefits to our lives throughout different fields including healthcare, defense, agriculture and transportation, where interconnected “intelligent” sensors communicate seamlessly over the internet. As IoT devices become more widespread, massive amounts of data are being generated by the hour and sent to the cloud which leads to several problems in terms of network congestion, slower connection and increased power consumption. This suggests that future IoT devices need to be smarter such that they are able to make decisions rather than just send data to the cloud. Smarter devices suggests that smarter electronic devices need to be integrated including smart memory devices that can sense, which will be the focus of this talk.

71-2: Effect of Measurement Temperature on the Charge Transport Behavior in Temperature Sensitive Ferroelectric Dielectric-Based Organic Field-Effect Transistors (Oral)
Start Time: 03:00 PM (15 Mins)
Speaker/Author: Samik Mallik, Shiv Prakash Verma, Subharthi Saha, Richeek Nayak and Prasanta Kumar Guha (Indian Institute of Technology Kharagpur, India); Dipak Kumar Goswami (IIT KHARAGPUR, India)
Presenter: Samik Mallik

Abstract: This paper emphasized the charge transport mechanism of a low-powered OFET fabricated using barium titanate (BaTiO3) nanocrystal as the dielectric material. These OFET-based devices are highly stable in air and exhibited the highest carrier mobility of 1.4 (±0.04) cm 2 /Vs. In general, high temperature processing of BaTiO3 proclaims excellent ferroelectricity due to the ABO3-type perovskite structure. However, the approach towards the very low temperature synthesis of BaTiO3 displayed a hexagonal phase in an amorphous matrix. The inclusion of hexagonal barium titanate nanocrystals (h-BTNCs) significantly lowered the surface roughness of the entire bi-layer dielectric system. An extensive temperature-dependent study ranging from 50K to 350K has been

carried out, and the variation of carrier mobility follows the Arrhenius behavior over the temperature range, supporting the hopping assisted charge carrier transport. Interestingly, two distinct regions are seen over the Arrhenius plot. This phenomenon has been explained by the structural phase change of h-BTNC at around 138 K, reflected in the large threshold voltage shift with temperature. Furthermore, we have calculated the activation energies for the temperature range of 150 K<T<300 K, and obtained the value of 9.47 meV, which reduces to 3.44 meV for 25 K<T<125 K. Such observation has been explained in terms of different charge transport mechanism at the grain boundaries.

71-3: Flexible organic electronic devices in healthcare for remote patient monitoring (Invited Talk)
Start Time: 03:15 PM (30 Mins)
Speaker/Author: Prof. Dipak K. Goswami, Indian Institute of Technology Kharagpur
Presenter: Prof. Dipak K. Goswami

Abstract: With the devastating COVID-19 pandemic spreading during the last two years, the need for smart-healthcare technology to take off the pressures of health professionals and provide the patient with much comfortable yet remote monitoring medical devices becomes paramount. Aligning the flexibility of organic electronic device-based sensors has been found to provide opportunities to develop wearable medical technology, including various diagnostic interventions to replace the existing gold standards with portable, affordable, and wearable medical devices with remote monitoring capabilities. In this talk, I will take on the development of a diagnostic intervention of pulmonary disfunction-related diseases, such as chronic obstructive pulmonary diseases (COPD) and sleep apnea, using a flexible organic field-effect transistors-based sensor system.

Session No: 72 | Session Title: Metal Air Batteries and Hybrid Energy Storage Systems

Audi: 6 | 02:30 PM-04:30 PM | **Session Chair:** Dr. Aiswarya Bhaskar
Track: Energy Storage and Batteries (ESB)
Date: 14-Dec-22

72-1: Interfacial Stabilization of Electrode Materials for Energy Storage (Invited Talk)
Start Time: 02:30 PM (30 Mins)
Speaker/Author: Prof. Malachi Noked, Bar-Ilan University
Presenter: Prof. Malachi Noked

Abstract: Understanding fundamental degradation mechanisms of electrode materials (EMs) , and their mitigation strategies, are challenged by constraints of the liquid electrolyte environment and the complexity of electrode/electrolyte interphase formation, namely the solid electrolyte interphase (SEI) layer which forms, grows, and changes (on the electrode interface) with battery usage. In my talk I will demonstrate how surface modification significantly suppress the degradation of the battery components (e.g. electrodes, and electrolyte) and facilitates long-term stability of the electrochemical device.
I will demonstrate how in our lab, we modify the surface of the EMs by either thin protection layer applied on its interface (using atomic layer deposition- ALD), or by surface reduction of high voltage cathode materials.

72-2: Role of Singlet Oxygen Quencher in Recharge Overpotential for Nonaqueous Li-Air Batteries (Oral)
Start Time: 03:00 PM (15 Mins)
Speaker/Author: Akhila S and Naga Phani B Aetukuri (Indian Institute of Science, India)
Presenter: Akhila S

Abstract: Aprotic Li-air batteries have gained enormous attention due to their high specific energy. However, while not compromising on rechargeability, the practical realization of the theoretically possible high specific energies has been elusive. Here, we use a singlet oxygen quencher, DABCO, and study the changes in recharge overpotential and parasitic reactions using a combination of galvanostatic charge-discharge measurements and gas analysis via Differential Electrochemical Mass spectrometry (DEMS). We find that the presence of quencher lowers the recharge overpotential. Interestingly, the higher concentration of quencher mediates electrolyte degradation and reduces oxygen evolution efficiency. Our results imply that a better understanding of the mechanisms and identifying stable additives that minimize parasitic chemistry during cell operation will be critical for rechargeable metal-oxygen batteries.

72-3: Development and Optimization of Highly Piezoelectric BTO/PVDF-TrFE Nanocomposite Film for Energy Harvesting Application (Oral)
Start Time: 03:15 PM (15 Mins)

Speaker/Author: Sandeep Singh Chauhan, Nadeem Tariq Beigh and Dibyajyoti Mukherjee (Indian Institute of Technology Delhi, India); Dhiman Mallick (IIT Delhi, India)
Presenter: Sandeep Singh Chauhan

Abstract: The interest in flexible vibrational energy harvesters is continuously increasing due to their low cost, biocompatibility, and environmental friendliness. This paper presents the optimization of PVDF-TrFE nanocomposite thin film in which barium titanate (BTO) is added as a functional material for the transformation of inherent α to highly piezoelectric β phase. The PVDF-TrFE and BTO are dispersed in dimethyl sulfoxide (DMSO) and spin-coated on a Molybdenum/polyethylene terephthalate sheet (Mo/PET). The composition and crystallinity are varied to optimize the growth of PVDF-TrFE and BTO/PVDF-TrFE films. X-ray diffraction (XRD) is used to characterize the spin-coated films' β phase. The field emission scanning electron microscope (FE-SEM) is utilized to characterize the film's uniformity. The Fourier Fourier-transform infrared spectroscopy (FTIR) is used to detect the transmittance in the wavenumber range from 400 to 1500 cm-1 of spin-coated BTO/PVDF-TrFE thin films. The piezo response force microscopy (PFM) measurement of films with different weight % and compositions is performed to identify the energy harvesting ability. It is found that the film deposited with 15% BTO in 15% PVDF-TrFE shows the best piezoelectric response. The piezoelectricity coefficient (d31) is found to be 1.29 nm/V, showing the excellent ability of polymer film to harvest vibrational energy available in the environment.

72-4: Lithium Voids Precede Dendrite Growth in Solid State Lithium Metal Batteries (Invited Talk)
Start Time: 03:30 PM (30 Mins)
Speaker/Author: Prof. Naga Phani B Aetukuri, Indian Institute of Science Bangalore, India
Presenter: Prof. Naga Phani B
Abstract: Solid-state lithium metal batteries (SSLMBs) that utilize metallic lithium as an anode offer high energy density and potentially long cycle and calendar life. However, stable plating and stripping of lithium in cells employing inorganic solid electrolytes, especially at current densities >0.2 mA/cm2, has been a challenge. In this talk, we will discuss the origins of dendrite growth in SSLMBs employing inorganic solid-state electrolytes. We show that there is a strong correlation between the onset of dendrite growth and the observation of lithium voids at the interface with the solid electrolyte. We discuss the properties of interlayers and propose descriptors for identifying interlayers that could further increase the current densities for cycling lithium without the undue necessity for high stack pressure.

72-5: Engineered Carbon Materials for Sodium Ion Hybrid Capacitors (Invited Talk - Withdrawn)
Start Time: 04:00 PM (30 Mins)
Speaker/Author: Prof. M M Shaijumon, Indian Institute of Science Education & Research Thiruvananthapuram
Presenter: Prof. M M Shaijumon

Abstract: Carbon materials, including carbon dots, carbon nanotubes, graphene, graphite, hard carbon, etc., have received greater attention due to their diversity, abundance, and favourable properties. The properties of carbon materials are easily tunable by doping with other elements or making composites with other materials.1 The unique chemical and structural features allow the possibility of engineering these materials, thus offering them unlimited advanced applications in energy storage and conversion.2 Here, efficient strategies to synthesise porous and hard carbon materials with significantly improved surface area and porosity features are explored for their applications in hybrid ion capacitors (HICs).3 For instance, engineered carbon samples with ‘open’ and ‘closed’ pores are synthesised to explore the sodium charge storage mechanism in hard carbon anodes. In-depth studies using different physicochemical techniques revealed strong evidence for adsorption/insertion-pore filling mechanism.4 The talk will also highlight our recent efforts on mass balancing of hybrid ion capacitor electrodes that could be employed as a design tool to guide the selection of optimized HIC devices for the intended applications.5

References
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Session No: 73 | Session Title: RF/mmwave/THz Devices and Circuits
Audi: 7 | 02:30 PM-03:45 PM | **Session Chair:** Dr. Eric Desbonnets
Track: RF, Millimeter and THz Technologies, Circuits and Systems (RF-THz)
Date: 14-Dec-22

73-1: On-chip Acceleration of Radio Frequency Machine Learning Models (Invited Talk)
Start Time: 02:30 PM (30 Mins)
Speaker/Author: Prof. Saibal Mukhopadhyay, Georgia Institute of Technology
Presenter: Prof. Saibal Mukhopadhyay
Abstract: The machine learning (ML) models have gained significant attention for radio frequency (RF) applications. However, incorporation of these models in a wideband RF system pipeline faces intriguing challenges to satisfy requirements of low processing latency and high processing throughput under the constraint of low processing power. This talk will discuss algorithm-hardware co-design methods for energy-efficient accelerations of RFML models using automatic modulation classification task as a case-study. First, we will discuss a quantization-aware accelerator design methodology to improve maximum throughput and power-efficiency of AMC model. Second, we will discuss hybrid processing pipeline that couples signal processing and machine learning to further improve ML models for AMC. Third, we will discuss potential of in-memory computing in RFML accelerations. The talk will conclude with discussions of future research directions in this field.

73-2: System Budgeting to System Realisation - A 22nm FDSOI 5G mmWave Front-End Module (FEM) Perspective (Oral)
Start Time: 03:00 PM (15 Mins)
Speaker/Author: Manshu Bishnoi, Ritabrata Bhattacharya and Vikas Aggarwal (Cadence Design Systems, India); Taranjit Kukal (Cadence, India); Jonathan Smith (Cadence, USA); Sankaran Aniruddhan (Indian Institute of Technology Madras, India)
Presenter: Manshu Bishnoi

Abstract: A comprehensive top-down system design methodology is presented and supported with a design of a Front-End Module (FEM) for 5G mobile applications targeting 24GHz-29GHz. While adopting package and PCB floor-planning and thermal challenges early in the design, a link budget analysis of a FEM in a system simulator followed by an implementation in GlobalFoundries' 22nm FDSOI process is reported with a focus on novel architectures to address system constraints. The FEM shows an excellent correlation between simulations and measurements and is further characterized post silicon by applying actual 5G signals in a real-time measurement mimicked simulation environment. A unified environment for co-designing and analysing the IC and package system is also described.

73-3: Enabling Technologies for Low-Cost mmWave SATCOM Terminals (Invited Talk)
Start Time: 03:15 PM (30 Mins)
Speaker/Author: Dr. Harish Krishnaswamy, Sivers Semiconductors
Presenter: Dr. Harish Krishnaswamy

Abstract: mmWave 5G has received a lot of attention due to its ability to deliver extremely high data rates to the user, while also posing challenges to the designer related to the need for large-scale arrays, high-power and high-efficiency power amplifiers, and advanced mmWave packaging. However, over the past year or two, there has been a significant rise in the interest in mmWave SATCOM, driven by the lowering of the barrier to launch satellites into orbit. SATCOM ground terminals, however, pose challenges that are akin to those posed by 5G on steroids - the arrays are 10x larger in size, amplifier efficiency is even more important, <2dB LNA noise figure is required, and electromagnetic, mechanical and thermal packaging challenges are even more severe. This presentation will touch upon various enabling technologies for mmWave SATCOM ground terminals - RF-SOI technologies, high-power high-efficiency mmWave PA design, extremely-low-NF LNA design, and scalable multi-beamforming.

Session No: 74 | Session Title: Other Emerging Devices & Compute Technology - 3
Audi: 8 | 02:30 PM-04:15 PM | **Session Chair:** Prof. Shubham Sahay
Track: Other Emerging Devices & Compute Technology (EDCT)
Date: 14-Dec-22

74-1: Transient memory and learning in correlated oxide neuromorphic devices (Invited Paper)
Start Time: 02:30 PM (30 Mins)

Speaker/Author: Sandip Mondal (Indian Institute of Technology Bombay & Purdue University, India); Ravindra Singh Bisht, Chengyang Zhang and Shriram Ramanathan (Purdue University, USA)
Presenter: Sandip Mondal

Abstract: Biological neural systems can learn and forget information that is one possible mechanism for stability and lifelong learning of neural circuits. Emulating such features in electronic devices is essential for advancing neuromorphic electronics. We discuss examples of memory devices using strongly correlated oxides to illustrate learning behavior in this conference proceeding. We give examples of transient memory and forgetting dynamics by controlling the strength of the electrical stimuli as well as stochastic behavior. Using examples of prototypical Mott insulators such as NiO and VO2, we present our vision for a neuromorphic platform utilizing quantum materials. The studies inform design of electronic hardware in emerging AI and can in future be extended to brain-machine interfaces.

74-2: From Enhanced Responsivity to Deep Sensing: Advances in Light Detection (Invited Talk)
Start Time: 03:00 PM (30 Mins)
Speaker/Author: Prof. Doron Naveh, Bar-Ilan University, Israel
Presenter: Prof. Doron Naveh

Abstract: The emergence of 2D layered compounds has ameliorated the fields of electronic and optoelectronic devices and are considered as a promising platform for the developments of devices in the quantum era. To list a few examples, this progress has included the demonstrations of ultrafast photodetectors, room-temperature mid-infrared photodetection, and electrical tunable spectral response by Stark effect. In this talk the recent progress on combined trajectories will be discussed – including fast, room temperature short wave infrared detection of hot photo carriers by intercalated MoS2 and a few examples on the electrical control of spectral response in photodetectors of 2D materials and heterostructures. Finally, the use of computational resources for the performance of spectral measurements, termed “Deep Sensing”, will be shortly reviewed.

References
[1] A. Twitto et al. ACS Nano 2022 https://doi.org/10.1021/acsnano.2c07347
[2] C. Stern et al. Advanced Materials 2021 https://doi.org/10.1002/adma.202008779
[3] S. Yuan et al. Nature Photonics 2021 https://doi.org/10.1038/s41566-021-00787-x

74-3: Spin Orbit Torque Tunable Skyrmion Neuromorphic Devices (Oral)
Start Time: 03:30 PM (15 Mins)
Speaker/Author: Aijaz Hamid Lone (KAUST - Thuwal & King Abdullah University of Science and Technology, Saudi Arabia); Xuecui Zou and Glen Isaac Maciel Garcia (KAUST - Thuwal, Saudi Arabia); Xiaohang Li (KAUST, Saudi Arabia); Hossein Fariborzi (King Abdullah University of Science and Technology, Saudi Arabia)
Presenter: Aijaz Hamid Lone

Abstract: Skyrmionic devices are promising candidates for energy efficient and highly integrated data storage and computing applications, owing to their small size, topological protection, and low drive current. In this abstract we propose novel spin orbit torque (SOT) controlled skyrmion device structures and their application in neuromorphic computing. We propose a spin orbit torque-driven SOT skyrmion magnetic tunnel junction (MTJ) device showing Leaky Integrate and Fire (LIF) neuron behaviour, and a SOT-controlled MTJ synaptic device in which the skyrmion size depends on the thickness of the free layer. Furthermore, we implement the spiking neural network and artificial neural network based on these devices for MNIST data classification.

74-4: Development of Ga2O3 devices and diodes towards converter applications at AFRL (Invited Talk)
Start Time: 03:45 PM (30 Mins)
Speaker/Author: Dr. Andrew Green, Air Force Research Laboratory, United States
Presenter: Dr. Andrew Green

Abstract: Ga2O3 device development has seen rampant progress over the past decade due to the combination of the availability of high quality substrates, epitaxial doping capabilities and the material’s field strength. This talk will discuss process modules which has enabled high DC conduction loss and dynamic switching loss figures of merit. Key process modules include gate scaling, implantation optimization, self-aligned processes and dielectric optimization.

Session No: 75 | Session Title: Atomistic Modelling and Simulation
Audi: 9 | 02:30 PM-04:15 PM | **Session Chair:** Prof. Avirup Dasgupta
Track: Modelling and Simulations (MS)
Date: 14-Dec-22

75-1: Ab-initio modeling of magneto-electronic devices (Invited Paper)
Start Time: 02:30 PM (30 Mins)
Speaker/Author: Sabyasachi Tiwari (UT Austin, USA); Maarten Van de Put (Imec, Belgium); Bart Soree (Imec, India); William G Vandenberghe (University of Texas at Dallas, USA)
Presenter: Sabyasachi Tiwari
Abstract: We present a first-principle based computational framework to model low-dimensional magnetic materials and their magnetization dynamics. We apply our method first on well-known 2D magnetic materials such as CrI3 and CrBr3. Next, we apply our method on transition metal doped 2D transition-metal dichalcogenides (TMDs). Finally, as an example of our device modelling methodology, we model a magnetic memory device using an interface between a 2D topological insulator and a 2D FM and show that a very fast switching of magnetic domain is possible in such devices (a fast write operation).

75-2: Analysis of Electronic Waveguide Bends in Graphene Subject to Dirac Point Fluctuations (Oral)
Start Time: 03:00 PM (15 Mins)
Speaker/Author: Emile Vanderstraeten and Dries Vande Ginste (Ghent University, Belgium)
Presenter: Emile Vanderstraeten

Abstract: Various optics-inspired electronic devices based on graphene have been proposed, owing to the linear dispersion relation of the charge carriers. In this contribution, the waveguide bend is examined by means of a higher-order time-domain method for the (2+1)D Dirac equation and it is demonstrated that, because of the peculiar properties of graphene, sharp waveguide bends with low losses are achievable even when Dirac point fluctuations are taken into consideration.

75-3: Extremely Scaled Silicon Nanosheet Transistors (Oral)
Start Time: 03:15 PM (15 Mins)
Speaker/Author: Keshari Nandan (IIT-Kanpur, India); Amit Agarwal, Somnath Bhowmick and Yogesh Chauhan (Indian Institute Of Technology, India)
Presenter: Keshari Nandan

Abstract: The nanosheet MOSFETs' architectures are considered to be the most promising candidates for the sub-3/5 nm technology node, owing to their strong immunity to short-channel effects (SCE). In these structures, quantum confinement effects are crucial, and full-band quantum transport simulations are adequate to capture these confinement effects accurately. Here, we assess the performance limit of ultra-scaled Si nanosheet n-MOSFETs through full-band quantum transport simulations. We consider five highly scaled Si nanosheets of different widths (<3.5 nm) and different thicknesses (< 1.5 nm). Also, we scale the gate length down to a few nanometers to study the limiting performance in ultra-scaled devices.

75-4: Estimation of Temperature Rise in an Atomically Separated Plasmonic Dimer Under Resonant Optical Illumination (Oral)
Start Time: 03:30 PM (15 Mins)
Speaker/Author: Priyanka Suri, Preeti Deshpande and Ambarish Ghosh (Indian Institute of Science, India)
Presenter: Priyanka Suri

Abstract: Plasmonic nanostructures have been engineered and investigated for their ability to confine light to sub-nm gaps and increase absorption[1]. The heat generated upon optical illumination of these nanostructures has been utilized in various applications ranging from biomedical technology to optoelectronics [2-5]. Here we computationally quantify the heat generated by one such sub-nm spaced plasmonic dimer geometry with monolayer MoS2 sandwiched in between. Such structures can be used for on demand material phase transformation and other optoelectronic applications[7]. This rise in local temperature confined to few nanometers has potential to be used as optically controlled nano heaters for heat assisted storage and patterning.

75-5: Temperature Dependent Band Gaps and Giant Excitonic Binding Energies in Novel 2D beta-phase Nitrogen Arsenide and Nitrogen Antimonide (Invited Talk)
Start Time: 03:45 PM (30 Mins)
Speaker/Author: Dr. Sitangshu Bhattacharya, Indian Institute of Information Technology-Allahabad, India

Presenter: Dr. Sitangshu Bhattacharya

Abstract: We present a detailed study of the electronic and optical properties of two new monolayer materials, nitrogen arsenide NAs, an nitrogen antimony NSb in their beta-phases. We used a combination of advanced many-body techniques to study electron–electron, electron–hole, electron–phonon, and even exciton–phonon interactions, leading to unique descriptions and deciphering of extraordinary properties of materials under investigation. Both wide-gap semiconductors, NAs and NSb (indirect quasiparticle gap ~4.5 and ~3.7 eV, respectively), embody strong exciton binding energies, ~1.6 and ~1.4 eV, respectively. In opposite, finite-temperature optical absorption in NSb is quite resilient to the temperature variations. We further proved that even a small tensile biaxial strain stabilizes with no loss in absorbance spectra; therefore, the practical preparation of them on support or included in heterostructures is possible.

Session No: 76 | Session Title: Specialized sources - Lasers & LED
Audi: 10 | 02:30 PM-04:15 PM | **Session Chair:** Prof. Kausik Majumdar
Track: LED & Semiconductor Lasers: Device, Physics & Modules (LL)
Date: 14-Dec-22

76-1: Advances in Optical Vortex Lasers (Invited Talk) (Invited Talk)
Start Time: 02:30 PM (30 Mins)
Speaker/Author: Prof. Jian Wang, Wuhan National Laboratory for Optoelectronics, Huazhong University of Science and Technology, China
Presenter: Prof. Jian Wang
Abstract: In this invited talk, we will introduce recent advances in optical vortex lasers, including reconfigurable and tunable twisted light laser, metasurface-assisted orbital angular momentum carrying Bessel-Gaussian laser, integrated high-speed directly modulated cylindrical vector beam laser, and all-fiber wavelength-switchable orbital angular momentum laser assisted by fiber Bragg grating and Fabry-Perot interferometer directly inscribed in erbium-doped fiber with femtosecond laser. Finally, we will also discuss future perspectives of optical vortex lasers.

76-2: Polariton lasers in organic molecular materials (Invited Talk)
Start Time: 03:00 PM (30 Mins)
Speaker/Author: Prof. Vinod Menon, City College & Graduate Center Cuny
Presenter: Prof. Vinod Menon,

Abstract: Exciton-polaritons, half-light half-matter quasiparticles that form in optical cavities have become a highly attractive candidate to realize Bose Einstein like condensates in the solid state that emit coherent radiation. Also called polariton lasers, these systems show lower threshold than the more conventional photon lasers because they do not need population inversion. Organic molecules have emerged as an appealing system to realize polariton lasers owing to their ability to operate at room temperature. Following a brief introduction to polariton lasers, I will present our recent work on realizing a universal platform for achieving polariton lasing using commercially available dyes using a small molecule ionic isolation lattice (SMILES) host. Possibility to realize lattices of polariton lasers and their potential as analog Hamiltonian simulators will also be discussed.

76-3: InP/ZnS Core Shell Quantum Dots as Temperature Sensor (Oral)
Start Time: 03:30 PM (15 Mins)
Speaker/Author: Barnali Mahato, Palash Kusum Das and Asha Bhardwaj (IISc Bangalore)
Presenter: Barnali Mahato

Abstract: We report the synthesis of high-quality, non-toxic, highly emitting InP/ZnS core-shell QDs. The QDs exhibit photoluminescence that is temperature dependent. A planar configuration of QDs has been used to fabricate a temperature sensor.

76-4: New market segments enabled by far-UVC technologies (Invited Talk)
Start Time: 03:45 PM (30 Mins)
Speaker/Author: Prof. Nicolas Volet, UV Medico, Denmark
Presenter: Prof. Nicolas Volet

Abstract: Part of the ultraviolet spectrum from 200 nm to 230 nm wavelength, called far-UVC, is highly absorbed by proteins in the superficial inactive cells of the skin and eyes. This allows for direct exposure of far-UVC at effective doses for pathogen deactivation.

UV Medico develops and produces far-UVC solutions. Our products have the advantage of being suitable for continuous disinfection of both the air and surfaces in occupied spaces. As such, far-UVC has a broader application area than conventional germicidal UV light sources which damage living cells. The latter are restricted to applications without direct human exposure, such as upper room ventilation systems and disinfection robots. Research on far-UVC has recently triggered a movement to increase exposure limits and adapt regulations accordingly. With the progressive adherence of regulatory agencies, new applications are enabled. This presentation will focus on the food industry as an example of the diverse application field.

Session No: 77 | Session Title: Novel devices for Neuromorphic Computing
Audi: 11 | 02:30 PM-04:00 PM | **Session Chair:** Prof. Debanjan Bhowmik
Track: Neuromorphic Device Technology, Circuits and Systems (NDTCS)
Date: 14-Dec-22

77-1: Design of Spintronics-Based Neuronal and Synaptic Devices for Spiking Neural Network Circuits (Invited Paper)
Start Time: 02:30 PM (30 Mins)
Speaker/Author: Debasis Das, Yunuo Cen, Jianze Wang and Xuanyao Fong (National University of Singapore, Singapore)
Presenter: Debasis Das

Abstract: Topologically stable magnetic skyrmion has a much lower depinning current density that may be useful for memory as well as neuromorphic computing. However, skyrmion-based devices suffer from the Magnus force originating from the skyrmion Hall effect, which may result in unwanted skyrmion annihilation if the magnitude of the driving current gets too large. A design of an artificial neuron and a synapse using a synthetic antiferromagnetically coupled bilayer device, which nullifies the Magnus force, is demonstrated in this work. The leak term in the artificial leaky integrate-and-fire neuron is achieved by engineering the uniaxial anisotropy profile of the neuronal device. The synaptic device has a similar structure as the neuronal device but has a constant uniaxial anisotropy. The synaptic device also has a linear and symmetric weight update, which is a highly desirable trait of an artificial synapse. Neuronal and synaptic devices based on magnetic domain-wall (DW) motion are also studied and compared to skyrmionic devices. Our simulation results show the energy required to perform such operation in DW or skyrmion-based devices is on the order of a few fJ.

77-2: Al/Lu/Lu2O3/Al Memristor for Synaptic and Memory Applications (Oral)
Start Time: 03:00 PM (15 Mins)
Speaker/Author: Maryala Praveen (National Institute of Technology - Warangal, India)
Presenter: Maryala Praveen

Abstract: In this paper, we propose the designing of bipolar resistive switching Memristor using high-k dielectric material ‘Lu2O3' as switching layer using combined software package of COMSOL multi-physics package tool based on Finite element method (FEM). The simulation results of Lu2O3 memristor reports a stable hysteresis I-V characteristics and observed lower C2C variability of 13.61% and 14.54% for SET and RESET states respectively which noted lower values than earlier high-k dielectric Y2O3 memristor and also observed ‘Potentiations' and ‘Depressions' of synaptic weights with different Voltage ramp-rates for synaptic applications and CQ behavior phenomenon enhances the device for multi-level storage and high-density memory applications.

77-3: A Robust-Compact Model to Imitate the Neuronal Dynamics With 2T Based FeFET-MOSFET Capturing Temperature Effects (Oral)
Start Time: 03:15 PM (15 Mins)
Speaker/Author: Rameez Raja Shaik and L Chandrasekar (IIITDM Kancheepuram, India); V Rajakumari (Indian Institute of Information Technology Design and Manufacturing, Kancheepuram, India); Kumar Pradhan (Indian Institute of Information Technology Design and Manufacturing Kancheepuram, India)
Presenter: Rameez Raja Shaik

Abstract: In this work, a robust-compact model based on 2T-ferroelectric FET (FeFET)-MOSFET oscillator based spiking neurons is developed and investigated for external temperature effects. The compact model is rigorously tuned and validated to existing literature for improving the accuracy of investigations. Emulation of neurons that can exhibit both the excitatory and inhibitory dynamics that are typically shown in cortical neurons. The compact model is tuned to reliably mimic regular spiking type cortical neurons with Zr-doped HfO 2 (HZO) and Si-doped HfO 2 (HSO) based FeFET(s). The analytical simulations has shown alterations at FeFET

oscillations and no visible changes in the digital spikes output for the regular spiking type cortical neurons dynamics.

77-4: Manganite based RRAM for Stochasticity Control for Boltzmann Machine (Invited Talk)
Start Time: 03:30 PM (30 Mins)
Speaker/Author: Prof. Udayan Ganguly, IIT Bombay
Presenter: Prof. Udayan Ganguly

Abstract: Non-filamentary manganite-based RRAM provides richness in behavior & controls due to the interplay of ionic, thermal, and electron conduction. We have shown that set & reset processes are enabled by positive vs. negative feedback leading to polarity-controlled stochastic vs. deterministic switching. The stochastic set enables a probabilistic switching in a neuron for a Boltzmann Machine. The deterministic reset enables excellent HRS control which enables weight update. Further, it enables highly controlled initialization of the HRS state that produces a very controlled stochastic switching distribution that remains drift free over time. Such stationary distributions enabled by deterministic/stochastic device physics produces improved performance in NP-Hard graphical optimization problems like maximum cut (Max-cut).

Session No: 78 | Session Title: Emerging phenomenon in 2D materials
Audi: 1 | 04:30 PM-06:00 PM | **Session Chair:** Prof. Prasana K Sahoo
Track: 2D Material Based Technologies (2DT)
Date: 14-Dec-22

78-1: Strain-driven quantum devices (Invited Talk)
Start Time: 04:30 PM (30 Mins)
Speaker/Author: Prof. Luis A Jauregui, University of California, Irvine, USA
Presenter: Prof. Luis A Jauregui

Abstract: Topological order and materials have been at the center of attention in condensed matter physics and engineering. Topological materials, a new quantum state of matter, are a family of quantum materials with boundary states whose physical properties are robust against disorder. Therefore, there have been few examples for a topological phase transition realized experimentally, even fewer cases for an in-situ tuning of the topological phase. For the first part of my talk, I will discuss our results and methods to apply uniaxial strain in topological van der Waals quantum materials and how it influences its electrical properties. Our results point towards a topological phase transition of the system tuned by in-situ uniaxial strain. For the second part of my talk, I will discuss our approach to creating dynamic strain in van der Waals quantum materials and how to control the electron and excitons dynamics in such systems. Our results could pave the way for engineering novel quantum devices as well as a step towards a solid-state quantum simulator platform.

78-2: Fabrication of EDLTs to Electrochemically Control Metal-Insulator Transition in VO2 (Oral)
Start Time: 05:00 PM (15 Mins)
Speaker/Author: Smrutirekha Mahapatra, Debasish Mondal and Naga Phani B Aetukuri (Indian Institute of Science, India)
Presenter: Smrutirekha Mahapatra

Abstract: Electron-electron interactions in transition metal oxides can enable novel macroscopic properties like metal-to-insulator transitions. Using such materials in field effect transistors can potentially enhance the current state-of-the-art devices by providing unique means to overcome their conventional limits. Deposition of high quality thin films and the device fabrication technique play an important role in the device response to an electric field. In this work, we present the deposition of high quality thin films of Vanadium dioxide (VO2) and a complete device fabrication protocol for an electric double-layer transistor (EDLT) using VO2 as the channel material. Further, we discuss the electric field-induced metal-to-insulator transition (E-MIT) in the VO2 thin film.

78-3: Strain Engineering in Transition Metal Dichalcogenide/Piezoelectric Thin Film Heterostructures (Oral)
Start Time: 05:15 PM (15 Mins)
Speaker/Author: Abin Varghese, Adityanarayan Pandey and Udayan Ganguly (Indian Institute of Technology Bombay, India); Nikhil V Medhekar (Monash University, Australia); Saurabh Lodha (Indian Institute of Technology Bombay, India)
Presenter: Abin Varghese

Abstract: Strain engineering has been employed as an effective methodology to tune the electrical properties of semiconductors like silicon and germanium. Likewise, for two-dimensional (2D) semiconducting materials, the effect of strain on the crystal structure has been a topic of significant interest in both electronic and optical aspects. In this work, we explore heterostructures of 2D materials with piezoelectric thin films to understand the effect of strain transfer from the piezoelectric film to the 2D material, here MoS2. Supported by our first principles-based density functional theory calculations, we experimentally demonstrate the tunability of electrical transport properties of MoS2 with strain. This strategy can be useful for improving the channel conductance and mobility values of 2D materials.

78-4: Tunable Many-body Interactions and Induced Superconductivity in a Helical Luttinger Liquid (Invited Talk)
Start Time: 05:30 PM (30 Mins)
Speaker/Author: Prof. Bent Weber, Nanyang Technological University
Presenter: Prof. Bent Weber

Abstract: The interplay of topology, superconductivity, and many-body correlations in 1D has become a subject of intense research for the pursuit of non-trivial superconducting pairing. The boundaries of atomically-thin topological insulators in 2D – amongst them the quantum spin Hall (QSH) insulator – provide a natural realisation of strictly 1D electronic structure with linear (Dirac) dispersion and spin-momentum locking (helicity).
We show that the topological edge states of the QSH insulator 1T'-WTe2 harbour a strongly correlated 1D electronic ground state – a helical Tomonaga-Luttinger Liquid (TLL) – whose many-body Coulomb interactions can be effectively controlled by the edge state's dielectric environment. This demonstrates tunability of a helical TLL in both its fundamental dependencies on potential and kinetic energy terms, respectively. Finally, we show that super-conductivity can be induced into the 1T'-WTe2 quantum spin Hall state by proximity-coupling to a superconducting van-der-Waals substrate, giving rise to an induced superconducting order parameter as large as 0.6meV in WTe2, stable beyond a B=2T magnetic field.

Session No: 79 | Session Title: Integrated Photonics - Components and Metamaterials
Audi: 2 | 04:30 PM-05:30 PM | **Session Chair:** Prof. Shailendra Varshney
Track: Integrated Photonics & Fibre Lasers (IPFL)
Date: 14-Dec-22

79-1: Active and lasing dielectric metasurfaces (Invited Paper)
Start Time: 04:30 PM (30 Mins)
Speaker/Author: Aditya Tripathi, Sergey Kruk and Yuri Kivshar (The Australian National University, Australia)
Presenter: Aditya Tripathi

Abstract: We combine the concepts of engineering the efficiency of light trapping (meta-photonics) and those of light matter interaction (engineering gain media) to demonstrate functioning active nanophotonic devices like lasers, light sources, and switchable devices.

79-2: Design and Fabrication of Hybrid Lithium Niobate Electro-Optic Modulators (Oral)
Start Time: 05:00 PM (15 Mins)
Speaker/Author: Viphretuo Mere, Forrest Valdez and Shayan Mookherjea (University of California San Diego, USA)
Presenter: Viphretuo Mere

Abstract: A process for designing and fabricating hybrid lithium niobate Mach-Zehnder electro-optic modulators is described. The design uses unetched thin-film lithium niobate bonded to a foundry-fabricated chip containing planarized silicon nitride waveguides. We demonstrate 3-dB electro-optic bandwidth greater than 110 GHz and VπL of 2.4 V.cm, at 1310 nm wavelength.

79-3: Low Pπ-Value Thermal Phase-Shifters in Si-Photonics Technology (Oral)
Start Time: 05:15 PM (15 Mins)
Speaker/Author: Shantanu Pal (GlobalFoundries Engineering Private Limited, India)
Presenter: Shantanu Pal

Abstract: A theoretical and experimental study has been carried out on thermal phase-shifters developed using silicon photonics technology. It has also been shown that Mach Zehnder Interferometer (MZI) structures

developed with sealed undercut thermal phase-shifters show lower value of P π (~7 mW) compared to MZI structures developed using standard thermal phase-shifters (P π ~32 mW) while both have waveguides with similar cross-sectional geometries. MZI structures developed with thermal phase-shifters were designed to guide only TE-polarized light over the O-band (1260-1360nm) and extended C-Band (1500-1600nm).

Session No: 80 | Session Title: GaN Device Technology & Physics
Audi: 3 | 04:15 PM-06:00 PM | **Session Chair:** Dr. Ritu Sodhi
Track: Wide Bandgap Power Semiconductor Technologies (WPSD)
Date: 14-Dec-22

80-1: Multiphysics Modeling of Wide Bandgap Devices (Invited Talk)
Start Time: 04:15 PM (30 Mins)
Speaker/Author: Prof. Swaroop Ganguly, IIT Bombay, India
Presenter: Prof. Swaroop Ganguly

Abstract: The design and analysis of electronic devices increasingly demand 'multi-physics' modeling. In this context, that most commonly means we have to incorporate the physics of thermal, mechanical or other effects in additional to the usual, viz. electron transport plus electrostatics. In this talk, I will go through the following three case studies, drawn from our work, on multi-physics simulation of wide bandgap semiconductor devices. First, the effects of substrate thinning on GaN HEMT performance. Second, the incorporation of mechanical strain for performance enhancement in SiC power MOSFETs. And third, the electro-thermal modeling of their short-circuit capability.

80-2: WBG Devices and it's application in power products (Invited Talk)
Start Time: 04:45 PM (30 Mins)
Speaker/Author: Mr. Milind Dighrasker, Infineon Technologies
Presenter: Mr. Milind Dighrasker

Abstract: The adoption of WBG in industry is rapidly increasing for power electronics systems. The choice of power train stage, topology, switching frequency etc. for WBG adoption, have been always a crucial decision points for system designers. This talk highlights few emerging systems where WBG adoption can make a large impact on system performance, features & power density. In this talk, few select systems power train & possible topologies for each stage of the power train will be analyzed. The impact of using WBG for each stage/topology will be analyzed by design examples.

80-3: Trends, Challenges and Solutions in Next Gen SiC/ GaN Power Devices Fabrication (Sponsored)
Start Time: 05:15 PM (15 Mins)
Speaker/Author: Mr. Peter Griffiths, Keithley (Tektronics)
Presenter: Mr. Peter Griffiths, Keithley (Tektronics)

Abstract: Quantum computing which was a theoretical conversation few years back, limited to imaginations of science fiction visionaries, is now gaining acceleration and investment from various applications and sectors. Quantum properties brings in various advantages over traditional computing as already demonstrated. The challenge is to scale these systems for useful computation. This paper will highlight some of the control challenges along with few unique methodologies and solutions to address the same.

80-4: EOS and ESD-related failures of GaN-based LEDs (Invited Talk)
Start Time: 05:30 PM (30 Mins)
Speaker/Author: Dr. Matteo Buffolo, University of Padova - Department of Information Engineering, Italy
Presenter: Dr. Matteo Buffolo, University of Padova - Department of Information Engineering, Italy

Abstract: Over the last decades, the reliability of GaN-based visible LEDs has vastly improved, mostly due to optimizations in device structure and in the epitaxial growth, to a point where a useful lifetime of the solid-state source in excess of 60 kh can be achieved. For these mature devices, extrinsic events, such as EOS and ESD events, represent a major lifetime-limiting factors during operation. This talk investigates from a physical standpoint the impact of overstress events on GaN-based LEDs, and reports on the device-level mitigation strategies that can be adopted to improve LED robustness against such phenomena.

Session No: 81 | Session Title: Challenges in Computing Systems
Audi: 4 | 04:30 PM-05:45 PM | **Session Chair:** Dr. Rahul Rao
Track: Advanced Logic Technologies (ALT)
Date: 14-Dec-22

81-1: Heterogeneous integration and chipletization in FPGAs (Invited Talk)
Start Time: 04:30 PM (30 Mins)
Speaker/Author: Mr. Praful Jain, AMD Inc., San Jose
Presenter: Mr. Praful Jain, AMD Inc., San Jose

Abstract: In the post-Moore's law era, scaling all I/Ps to the next process node is not always the best choice. In recent years, DTCO advancements have helped standard cells in achieving desirable PPA scaling, but SRAM cells and custom blocks have lagged behind. Today's FPGAs, like AMD Versal® ACAP (Adaptive Compute Acceleration Platform), are using more standard cell logic than ever before, but programmable fabric is still primarily made up of SRAMs and custom layouts. As a result, it is becoming more attractive to adopt some form of chipletization and heterogenous integration to drive future scaling of FPGAs.

81-2: Waferscale Computing (Invited Talk)
Start Time: 05:00 PM (30 Mins)
Speaker/Author: Dr. Saptadeep Pal, Auradine Inc., USA
Presenter: Dr. Saptadeep Pal

Abstract: Fueled by the tremendous growth of new applications in the domain of big-data computing, deep learning, and scientific computing, the demand for increasing system performance is far outpacing the capability of conventional methods for performance scaling. Traditionally, performance and energy scaling has relied on transistor and silicon scaling. However, developing chips, often very large ones in the advanced technology nodes, is becoming very challenging and costly. Moreover, system performance is often limited by inter-die connections. Today, dies with different functionality are packaged and integrated using PCBs. Unlike silicon features, package and PCB features have barely scaled (about 4-5x) over the past few decades. This severely limits performance and efficiency of processor systems. Traditional scale-out system building, and integration methodologies are failing to deliver the performance today's applications (such as artificial intelligence, big-data processing etc.) demand. As a consequence, future performance, power, and cost improvements cannot come from transistor technology alone. Then, how do we enable "System scaling"?

To target scale-out systems, we propose chiplet-based waferscale processors to dramatically reduce inter-die communication overheads. To that end, we developed the Si-IF technology where bare dies can be tightly integrated on a waferscale interconnect substrate to build scale-out processors up to a size of an entire wafer. However, building such a large consolidated waferscale system has its own challenges. For the first time, we explored the design space of waferscale power-delivery networks, cooling and trade-offs of yield and inter-GPM network topologies, etc. I will discuss some of these challenges and solutions that we developed to architect a large shared memory waferscale prototype system. Next, I will make a case for waferscale GPU and waferscale graph acceleration, where we leverage the massive bisection bandwidth and sub-1ns inter-die latencies to build high-performance computing systems. Our work shows that massive gains in excess of 5-10x can be achieved in terms of both performance gains as well as system energy using waferscale integration.

81-3: Industrial Safety in Semiconductor Industries (Sponsored)
Start Time: 05:30 PM (15 Mins)
Speaker/Author: Mr. Sato, Riken Keiki Co Ltd, Japan
Presenter: Mr. Sato

Abstract: Special gases used in process of Semiconductor manufacturing present hazard to plant and personnel equally. We will explain the dangers involved, solution to avoid them and methodology to sustain it. We will also discuss statutory regulations and accident case studies that help immensely in avoiding future hazardous situations. Our moto is to keep Semiconductor Industry Gas hazard free.

Session No: 82 | Session Title: RF/mmwave/THz Circuits and systems
Audi: 7 | 04:30 PM-05:45 PM | **Session Chair:** Dr. Mh. Rahman
Track: RF, Millimeter and THz Technologies, Circuits and Systems (RF-THz)
Date: 14-Dec-22

82-1: Millimeter Wave Power Amplifier Design (Invited Talk)
Start Time: 04:30 PM (30 Mins)
Speaker/Author: Dr. Hang LIU, Globalfoundries, Singapore
Presenter: Dr. Hang LIU

Abstract: Millimeter wave (mmWave) communication systems have attracted significant interest regarding meeting the capacity requirements of the future 5G network. Silicon power amplifier (PA) is one of the key challenging components due to high power efficiency and high energy efficiency requirements due to the inherent drawbacks of silicon processes, including low device speed, large losses, low supply, and breakdown voltages, etc. To overcome these issues, power-combining techniques are widely adopted to overcome the power limitation from a single-channel PA. Among different combining techniques, transformer power-combining provides good features such as wide bandwidth and compact size, and therefore is widely adopted. This talk reveals the evolution of mmWave PAs and present the latest power combiner designs.

82-2: Optimization of Carbon Fiber Loading in PDMS for Strong Microwave Absorption (Oral)
Start Time: 05:00 PM (15 Mins)
Speaker/Author: Gadadasu Chandana, Pritom J Bora and Praveen C Ramamurthy (Indian Institute of Science, India)
Presenter: Gadadasu Chandana

Abstract: Carbon fibers were reinforced in the poly dimethyl siloxane (PDMS) matrix, and composites of 2.5 wt %, 3 wt %, and 10 wt % concentration were effectively synthesized. The composite's complex relative permittivity values were measured, and microwave absorption properties were calculated for the synthesized PDMS composites. Based on the measured data, a data-driven approach was used to optimize the filler loading for efficient microwave absorption. It was observed that the composite's minimum reflection loss (RL) is about -51 dB for 0.3 wt % concentration at 2.9 mm thickness with an effective absorption bandwidth of 4.3 GHz in the Ku-band (12.4-18 GHz).

82-3: Low dimensional silicon and layered transition metal chalcogenides based THz detectors and modulators (Invited Talk)
Start Time: 05:15 PM (30 Mins)
Speaker/Author: Dr. Samaresh Das, Indian Institute Of Technology Delhi
Presenter: Dr. Samaresh Das

Abstract: The terahertz (THz) technology has been experienced rapid advancement in numerous potential applications in the last few years. This includes imaging, communication, material spectroscopy, security, and the bio-medical field. In the first part, a single silicon nanowire (NW) junctionless field-effect transistor (FET) based THz detector will be discussed. The maximum responsivity is observed around 0.425 THz, with a peak value of 468 V/W. Further, another class of THz detector employing type-II topological Dirac semimetal platinum telluride (PtTe2) has been manifested in the 0.1-1.5 THz frequency range. The broadband optical THz modulators will be covered in the 2nd part. These modulators are based on the new class of TMDs such as Platinum diselenide (PtSe2), Tantalum disulfide (TaS2), and Molybdenum disulfide (MoS2). The TMDs have been incorporated in the optical-controlled semiconductor-based THz modulators to improve modulation efficiency in modulation depth (~ 80%) and speed.

Session No: 83 | Session Title: Microfluidics and Bio-sensing
Audi: 8 | 04:30 PM-05:45 PM | **Session Chair:** Prof. Prosenjit Sen
Track: MEMS/NEMS and Heterogeneously Integrated Devices (NEMS)
Date: 14-Dec-22

83-1: A Xurography-Based Rapid Prototyping Method to Fabricate Low-Cost High Quality Metal Electrodes (Invited Paper)
Start Time: 04:30 PM (30 Mins)
Speaker/Author: Vinay Patel (Indian Institute of Technology Bombay, India); Peter Kruse and P. Ravi Selvaganapathy (McMaster University, Canada)

Presenter: Vinay Patel (Indian Institute of Technology Bombay, India); Peter Kruse and P. Ravi Selvaganapathy (McMaster University, Canada)

Abstract: Metal leaves are commercially available as thin films that have a thickness of approximately 100 nm. Metal leaves are used as low-cost conductive films on non-conductive materials. In past, metal leaves have been used on different non-conducting substrates to fabricate electrodes for various applications including sensing, and energy storage. However, most of these studies have either used unpatterned or indirectly patterned metal leaves. Here, a low-cost rapid xurography-based metal leaf patterning method is reported that has achieved a minimum line width of <100 micrometers. The patterned
metal leaves were characterized using scanning electron microscopy, white light interferometry and electrochemical techniques. The patterned metal leaves were used to fabricate electrochemical sensors and contact electrodes for chemiresistors.

83-2: Precise and Low Volume Sampling Using Microfluidic Device (Oral)
Start Time: 05:00 PM (15 Mins)
Speaker/Author: Nishant Kumar Sharma (Indian Institute of Science, India); Sen Prosenjit (IISc, India)
Presenter: Nishant Kumar Sharma

Abstract: We report a microfluidic device platform to precisely sample low volumes of fluids such as blood for disease diagnosis. It comprises a custom-engineered T-channel, a microfabricated PDMS device. The sampling rate (Q2) is controlled by the design of the sampling channels and the withdrawal rate (Q1) of continuous flow using a syringe pump in the main channel. Three devices with a flow rate ratio (Q1/Q2) of 10, 50, and 100 were designed and tested. The minimum experimental Q2 was found to be 160 nl/min against Q1 of 1.7 μl/min. The reported device has the capability to reduce the dead volumes, and precisely sample low volumes from regions where the sample volume is limited such as cerebrospinal fluid.

83-3: MICRO-NANO INTEGRATED SYSTEMS FOR LIFE SCIENCE APPLICATIONS (Invited Talk)
Start Time: 05:15 PM (30 Mins)
Speaker/Author: Prof. Muthukumaran Packirisamy, Concordia University, Montreal, Canada
Presenter: Prof. Muthukumaran Packirisamy

Abstract: In this presentation, we will talk about the in-situ synthesis of Au-PDMS and Ag-PDMS nanocomposites both at the macroscale and inside the channel of a microfluidic chip. The nanocomposite has been successfully used for sensing of antibody-antigen interactions, allowing the detection of various important proteins. Nanocomposites of metals integrated into other polymers such as PMMA, PVA, and PS have been synthesized as well by using UV, microwave and thermal reduction methods. The effect of the particle`s shape on the properties of nanocomposites and their sensing abilities has also been studied by synthesizing nanostar particles and integrating them into microchannels. Because of the biocompatibility and non-toxicity of gold and silver nanoparticles, their nanocomposites can be used for plasmonic detection of biological entities in cancer research.

Session No: 84 | Session Title: Multi-scale, 2D and Nanosheet Modelling

Audi: 9 | 04:15 PM-06:00 PM | **Session Chair:** Prof. Nihar Mohapatra
Track: Modelling and Simulations (MS)
Date: 14-Dec-22

84-1: Multi-scale modeling of devices based on two-dimensional materials heterostructures (Invited Talk)
Start Time: 04:15 PM (30 Mins)
Speaker/Author: Prof. Tarun Kumar Agarwal, IIT Gandhinagar, India
Presenter: Prof. Tarun Kumar Agarwal

Abstract: Atomically thin two-dimensional (2D) material-based devices have emerged as a possible successor of Si nanosheet transistors for future technology nodes. To continue scaling transistors on future technologies, we would need to transition to vertical carrier transport where the gate length does not pose a limitation in reducing the contacted gate pitch. Van der Waals (vdW) heterostructures based on 2D materials can facilitate the design of vertical transistors. This talk will discuss the multi-scale modeling technique to design and analyze vertical devices based on 2D materials heterostructures. The multi-scale modeling framework will include the atomistic modeling of vdW heterostructures to understand their electronic properties and vertical electron transport. Further, possible device designs will be discussed using a tight-binding Hamiltonian-based quantum transport framework.

84-2: Electrostatics of bulk versus nanoscale junctions (Invited Talk)
Start Time: 04:45 PM (30 Mins)
Speaker/Author: Dr. Vijaya Kumar Gurugubelli, IIT Tirupati
Presenter: Dr. Vijaya Kumar Gurugubelli

Abstract: Nanoscale devices based on atomically thin semiconductor layers, nanowires or nanotubes consist of PN junctions as either essential or parasitic elements. The mathematical treatment of the electrostatics of these junctions has been different for different geometries. We present a unified modelling approach based on a common set of approximations related to the electric field/potential distributions, and obtain simple analytical formulas for the depletion width, and the field and potential distributions. We show that the depletion width dependence on potential drop and inverse of doping varies from being square root in bulk to linear in atomically thin layers and exponential in nanowires/nanotubes. Further, we propose an effective medium theory, showing that an array of nanoscale junctions behaves as a bulk junction with effective permittivity and doping.

84-3: Analysis and Modeling of Leakage Currents in Stacked Gate-All-Around Nanosheet Transistors (Oral)
Start Time: 05:15 PM (15 Mins)
Speaker/Author: Manikandan Subramaniyan (Indian Institute of Technology-Roorkee, India); Nitanshu Chauhan (NIT-Srinagar, India); Navjeet Bagga (IIITPDPM Jabalpur, India); Abhishek Kumar (IIT Roorkee, India); Shashank Kumar Banchhor (Indian Institute of Technology Roorkee, India); Sourajeet Roy, Avirup Dasgupta and Anand Bulusu (IIT Roorkee, India); Sudeb Dasgupta (Indian Institute of Technology Roorkee, India)
Presenter: Manikandan Subramaniyan
Abstract: For efficient use of the upcoming Stacked Gate-all-around Nanosheet Field Effect Transistors (GAAFET), identifying and mitigating leakage current components are essential. This paper comprehensively investigates the leakage components not only in the nanosheets but also through the substrate, including effects such as Gate-Induced Drain Lowering (GIDL) and parasitic substrate leakage. We thoroughly investigate the impact of device geometry on the device leakage current and propose device design guidelines for mitigation of the substrate leakage current for these devices. In addition, we have modeled the GIDL current of GAAFETs using BSIM-CMG code.

84-4: Single Layer Substitution Doped Graphene FET: From Numerical Model to Extremely Closed-Form Region-wise Model and Application to Synaptic Plasticity (Invited Talk)
Start Time: 05:30 PM (30 Mins)
Speaker/Author: Dr. Kumar Prasannajit Pradhan, Indian Institute of Information Design and Manufacturing Kancheepuram
Presenter: Dr. Kumar Prasannajit Pradhan

Abstract: A phenomenological all region self-consistent drain current model for B/N substitution doped GFET is developed. The effects of B/N doping such as: shift in Dirac points and induced non-zero bandgaps are explicitly captured in this model. However, the self-consistent model only permits numerical solution and it requires precise initial assumption, which makes computationally exhaustive. Hence, a simplified region-wise potential-based analytical model is established for B/N doped GFET. The extreme closed-form analytical nature of region-wise model with computational efficiency makes it highly beneficial to establish a compact model for mimicking the device behavior in circuits. The synaptic devices based on B/N doped GFET have been modeled by utilizing the interface traps to manifest dynamic mimicking of synaptic plasticity.

Poster Session: 1 | Audi: 3 | **Date:** Dec. 12th, 2022 | **Time:** 07:00 PM-09:00 PM

Track: Energy storage and batteries (ESB)

P-1: Photo-Rechargeable Stable Metal Ion Batteries

Authors: Amar Kumar and Tharangattu Narayanan Narayanan (TIFR Hyderabad, India)

P-2: Zinc Incorporated 2D Nickel Cobalt Oxide Nano-Petals Based Electrode Material for High-Performance Supercapacitors

Authors: Sourav Karmakar (IIIT Kalyani, India); Sourish Haldar (JIS College of Engineering & Indian Institute of Information Technology Kalyani, India); Palash Chandra Maity (IIT Roorkee, India); Monojit Mondal (IIT KHARAGPUR, India); Rinky Sha (Indian Institute of Information Technology (IIIT) Kalyani, India); Indranil Lahiri (IIT Roorkee, India); Tarun K. Bhattacharyya (IIT Kharagpur, India)

P-3: Temperature Dependent Dielectric Properties of Spinel MgMn2O4 Nanofibers for LIB Anode

Authors: Abhinav Tandon, Shalu Rani and Yogesh Sharma (IIT Roorkee, India)

P-4: Metal Thiophosphates as a High-Capacity Cathode Material for Lithium Primary Battery

Authors: Syama Lenus (Xi'an Jiaotong University & Tata Institute of Fundamental Research. Hyderabad, India); Pallavi Thakur (Tata Institute of Fundamental Research Hyderbad, India); Sai Smruti Samantaray (Tata Institute of Fundamental Research Hyderabad, India); Tharangattu Narayanan Narayanan (TIFR Hyderabad, India); Dai Zhengfei (Xian Jiaotong University, China)

P-5: Enhanced Electrochemical Properties of Fe-Doped TiO2 Nanotubes for Supercapacitor Applications

Authors: Sarda Sharma (Amrita Vishwa Vidhyapeetham Bangalore Campus & BITS Pilani Hyderabad Campus, India)

P-6: Low-Cost Flexible Silk-Copper-Based Triboelectric Nanogenerator

Authors: Aditya Bhagavathi Kandala, Satish Bonam, Shiv Govind Singh and Siva Rama Krishna Vanjari (Indian Institute of Technology Hyderabad, India)

P-7: MWCNT/ZnIn2S4 Nanocomposite for Enhanced Photoelectrochemical Water Splitting Activity Under Visible Light Irradiation

Authors: Mohit Khosya, Mohd Faraz and Neeraj Khare (Indian Institute of Technology Delhi, India)

Track: Integrated Photonics & fibre lasers (IPFL)

P-8: A Hybrid Waveguide Bend Scheme for Low Footprint

Authors: Rahul K Dash (Indian Institute of Science Bangalore, India); Shankar Selvaraja (Indian Institute of Science, India)

P-9: Realistic Quantum Mechanical Modelling of Spontaneous Four-Wave Mixing in Silicon Nitride Waveguide and Ring Resonator

Authors: Asish Prosad (Indian Institute of Science, India); Rabindra Biswas (Indian Institute of Science Bangalore, India); Talabattula Srinivas (Indian Institute of Science, India); Varun Raghunathan (IISc, India)

P-10: An Integrated Tunable Delay Line for Photonic Computing on 45 nm CMOS Based Silicon Photonics Platform

Authors: Avijit Chatterjee and Riddhi Nandi (Global Foundries, India); Michal Rakowski and Abdelsalam Aboketaf (Global Foundries, USA); Mehrdad Djavid (Globalfoundries USA, USA)

P-11: External Probe-Based Amplified Spontaneous Emission in Cd1-xZnxSe/ZnSe Quantum Dots for Fiber Laser Application

Authors: Palash Kusum Das, Nishant Dhiman, Siva Umapathy and Asha Bhardwaj (IISc Bangaluru, India)\

Track: LED & semiconductor lasers: Device, physics & modules (LL)

P-12: Improvement in Performance of InGaN MQWs LEDs Using InxGa(1-x)N/ InyGa(1-y)N Chirped Quantum Barriers

Authors: Indrani Mazumder (AcSIR & CSIR-CEERI, India); Kashish Sapra (AcSIR, India & CSIR-CEERI, India); Harshita Aagiwal (CSIR CEERI, India); Manish Mathew and Ashok Chauhan (CSIR, India); Kuldip Singh (CSIR CEERI, India)

P-13: Effect of Indium Composition in Quantum Barrier on Performance of InGaN/InGaN Laser Diode Emitting at 410 nm

Authors: Kashish Sapra (AcSIR, India & CSIR-CEERI, India); Indrani Mazumder (AcSIR & CSIR-CEERI, India); Harshita Aagiwal (CSIR CEERI, India); Kamal Lohani (Solid State Physics Laboratory, DRDO, India); Dipendra Singh Rawal (Solid State Physics Laboratory, India); Ashok Chauhan (CSIR, India); Kuldip Singh (CSIR CEERI, India); Manish Mathew (CEERI Pilani, India)

P-14: Ambipolar Doping in Conjugated Polymer

Authors: Karandeep Singh (INDIAN INSTITUTE OF SCIENCE, India); Neha Chauhan, Aiswarya Abhisek Mohapatra and Satish Patil (Indian Institute of Science, India)

Track: Macroelectronics & Displays: devices, circuits & systems (DIS)

P-15: Strategy From the Fabrication of Polymer Thin Film Transistor on Rigid and Flexible Substrate to LTspice Simulation Towards Circuit Applications

Authors: Saiganesh Puttur and Soumya Dutta (Indian Institute of Technology Madras, India)

P-16: Temperature Control System for Fabrication of W-Microprobes

Authors: Abhishek Kumar, Saleem Ibne Hussain, Anirban Sardar and Santanu Talukder (IISER Bhopal, India)

P-17: Magnetron Sputtered Tungsten Oxide Films for Electrochromic Applications

Authors: Sudha Arumugam, Aarju Mathew Koshy, Faiz Ali, Parasuraman Swaminathan and Meenu Maria Solly (Indian Institute of Technology Madras, India)

P-18: Inkjet-Printed a-IGZO/Ag Schottky Diodes With >10^6 Rectification Ratio

Authors: Manvendra Singh (Indian Institute of Science, Bangalore, India); Jyoti Ranjan Pradhan (Indian Institute of Science, India); Subho Dasgupta (Indian Institute of Science (IISc), Bangalore, India).

P-19: Influence of Graphene Dispersion in P3HT-Based Thin Film Organic Field Effect Transistors

Authors: Ankit Malik, Ashutosh P and Bidisha Nath (Indian Institute of Science, India); Mayank Shrivastava (Indian Institute of Science Bangalore, India); Praveen C Ramamurthy (Indian Institute of Science, India)

P-20: Enhanced Thermoelectric Performance of Flexible n-Type Ag2Te-Nylon Composite Film for Thermoelectric Generator

Authors: Amish Kumar Gautam and Neeraj Khare (Indian Institute of Technology Delhi, India)

P-21: Effect of Light on the p-Type Doping of P3HT OFET by Oxygen

Authors: Shivangi Srivastava (IISc Bangalore, India)

P-22: Solution Processed High-k/Low-k Bilayer Gate Dielectrics for Flexible Organic Transistors

Authors: Sachin Rahi, Gargi Konwar and Shree Prakash Tiwari (Indian Institute of Technology Jodhpur, India)

Track: MEMS/NEMS and Heterogeneously Integrated Devices (NEMS)

P-23: Highly (111) Oriented Ti/Pt Thin Film on Si/SiO2 Substrates by DC Sputtering

Authors: Veeramani Thangavel, Antony Jeyaseelan A and Varadharajaperumal S (Indian Institute of Science, India)

P-24: Die Isolation Strategy for Suspended Devices Released by Dry Etching

Authors: Zareena Hassanbee (Indian Institute of Science, Bangalore, India); Goutam Prakash (Centre for Nano Science and Engineering (CeNSE), Indian Institute of Science, India); Sabiha Sultana (PES Institute of Technology & Indian Institute of Science, India)

P-25: A Simple and Cost-Effective Dual Side Lithography Alignment Process Using a Combination of a Single Mask and Direct Writing Double Exposure Process

Authors: Goutam Prakash (Centre for Nano Science and Engineering (CeNSE), Indian Institute of Science, India); Vasanth Kumar (Indian Institute of Science, Bangalore, India); Sabiha Sultana (PES Institute of Technology & Indian Institute of Science, India)

P-26: Flash Imaging for Microfluidics

Authors: Ishita Bansal (Indian Institute of Science Bangalore, India); Shamibrota Roy and Kaushik Basu (Indian Institute of Science, India); Sen Prosenjit (IISc, India)

P-27: Fabrication of Flexible Metglas Based Magnetic Energy Harvester Using PVDF-TrFE/KNN Composite Film

Authors: Sandeep Singh Chauhan and Maninder Kaur (Indian Institute of Technology Delhi, India); Nitika Batra, Madhusudan Singh and Bhaskar Mitra (IIT Delhi, India)

Track: Sensors and Bio-electronics (SBE)

P-28: Flexible ZnO Thin-Film Based Photosensor for Applications in Light-Induced Automation

Authors: Shivank Sahu (Indian Institute of Science Education And Research Bhopal, India); Lakhvir Singh and Mitradip Bhattacharjee (Indian Institute of Science Education and Research Bhopal, India)

P-29: IoT Based LPG, Smoke, Alcohol Detection System With Automatic Mains Cut-Off

Authors: Dwarakanath Dey (St. Thomas College of Engineering & Technology, India); Saikat Datta (St Thomas College Of Engineering & Technology, India); Subhojit Datta, Souptik Das and Tanusree Dutta (St Thomas College of Engineering and Technology, India)

P-30: Fabrication and Characterization of a Pyrolytic Carbon Film as a Quasi-Reference Electrode for Miniaturized Bioelectrochemical Applications

Authors: Pijus Kundu (CSIR-Central Electronics Engineering Research Institute (CEERI), India); Kashish Sapra (AcSIR, India & CSIR-CEERI, India); Indrani Mazumder (AcSIR & CSIR-CEERI, India); Beomsang Kim and Heungjoo Shin (Ulsan National Institute of Science and Technology, Korea (South))

P-31: Use of Novel Green Synthesized Co3O4-NPs for Electrochemical Sensing of Pb Ions

Authors: Simranjeet Singh (Indian Institute of Science, India); Pavithra N (INDIAN INSTITUTE OF SCIENCE, India); T S Sunil Kumar Naik (Indian Institute of Science, India); Radhika Varshney (Indian Institute of Science, Bangalore, India); Praveen C Ramamurthy (Indian Institute of Science, India)

P-32: Room Temperature Ozone Sensor Based on Indium Tin Oxide (ITO) Decorated Surface Acoustic Wave (SAW) Resonator

Authors: Jitendra Singh (CEERI Pilani, India); Saurabh Kumar Gupta and Vinita Vinita (CSIR-Central Electronics Engineering Research Institute Pilani, India)

P-33: VOCs Interaction With PANI/MoS2-Based Gas Sensor: Morphology Studies

Authors: Aakanksha Jain and Ajithkumar Mp (Indian Institute of Technology Kanpur, India); Siddharth Panda (India, India)

P-34: Printed PFPS Polymer Based CO2 Electrical Sensor With Schottky Diode Mathematical Modelling

Authors: Ramesh Babu Yathirajula (IIT Guwahati & Nanotechnology, India)

P-35: Polyaniline Based Dual Gate FET Gas Sensor

Authors: Shivam Kumar Gautam (Indian Institute of Technology Kanpur, India); Deepa Bhatt (IIT Kanpur, India); Shivam Nigam (Indian Institute of Technology, Kanpur, India); Siddharth Panda (India, India)

P-36: Live-Cell Imaging System Compatible With Magnetic Actuation in a Triaxial Helmholtz Coil

Authors: Paramita Modak, Reshma Vasantha Ramachandran, Ramray Bhat, Deepak K. Saini and Ambarish Ghosh (Indian Institute of Science, India)

P-37: Electro-Structured Cu Distorted Nanopyramids for Superior Sweat Glucose Sensing

Authors: Chiranjeevi Srinivasa Rao Vusa and Nachiket Aashish Gokhale (Indian Institute of Technology Kanpur, India); Siddharth Panda (India, India)

P-38: An Ultrasensitive and Selective PPY-fMWCNT Nanocomposite Electrical-Transducer Based Chemiresistive Immunosensing Platform for Early Detection of Alzheimer's

Authors: Patta Supraja and Rahul Gangwar (Indian Institute of Technology Hyderabad, India); Suryasnata Tripathy (Indian Institute of Information Technology Surat, India); Siva Rama Krishna Vanjari and Shiv Govind Singh (Indian Institute of Technology Hyderabad, India)

P-39: A Novel Technique to Realize a Flexible Tactile Sensor

Authors: Vikram Maharshi (Indian Institute of Technology, Delhi, India); Ajay Agarwal (IIT Jodhpur, India); Bhaskar Mitra (IIT Delhi, India)

Track: Solar cells & photodetectors: Physics, Device, & Modules (SP)

P-40: Analysis and Observations Into the Quantum Dot-Quantum Well Hybrid Structure Using a CZTSSe/CZTS

Authors: Chandrasekar Palanisamy and Soumyaranjan Routray (SRM Institute of Science and Technology, India)

P-41: Facet-Oriented Free-Standing Cs2AgBiBr6 Double Perovskite Microcrystals via Hot-Spin Casting Synthesis for Efficient Photodetection

Authors: Mozakkar Hossain, Md Sariful Sheikh and K. D. M. Rao Rao (Indian Association for the Cultivation of Science, India)

P-42: Steady State Electroluminescence Imaging of Perovskite Solar Cells

Authors: Jeykishan Kumar K (Central Power Research Institute, India); Bidisha Nath (Indian Institute of Science, India); Tulika Bhattacharjee (Central Power Research Institute, India); Praveen C Ramamurthy (Indian Institute of Science, India)

P-43: A Broad Range (UV-Visible-NIR) Photodetector Based on N-Doped CQD/MoS2 (0D/2D) Quantum Dimensional Heterostructure

Authors: Krishan Kumar (Indian Institute of Technology Roorkee, India); Davinder Kaur (Indian Institute of Technology Roorkee (IITR), India)

P-44: Dielectric Properties of Acetamidinium Substituted Methylammonium Lead Iodide Perovskite

Authors: Shubhangi Bhardwaj, Ashutosh Mohanty and Ranjan Das (Indian Institute of Science Bangalore, India); Pallavi Singh (Weizmann Institute of Science, Israel); Ankit Singh and Dipankar Das Sarma (Indian Institute of Science Bangalore, India); Sushobhan Avasthi (Indian Institute of Science & Centre for Nano Science and Engineering (CeNSE), India)

P-45: Doping-Induced Phase Transformation in All-Inorganic Perovskite CsPbI3 With Enhanced Structural and Optical Stability

Authors: Shaona Bose, Somnath Mahato, Baiydanath Roy, Arup Ghorai, Sanjeev Kumar Srivastava, Narayan Chandra Das and Samit Kumar Ray (Indian Institute of Technology Kharagpur, India)

P-46: Synthesis of Au-WS2 Hybrid Nanostructures for Performance Enhancement in Organic Solar Cells

Authors: Abhijith T and Rakesh Suthar (Indian Institute of Technology Delhi, India); Supravat Karak (IIT Delhi, India)

P-47: Role of Energetic Disorder in Energy Loss of Bulk Heterojunction Organic Solar Cells

Authors: Rakesh Suthar and Abhijith T (Indian Institute of Technology Delhi, India); Supravat Karak (IIT Delhi, India)

P-48: High-Performance Broadband Photodetector Based on a WS2-QD/Monolayer MoS2 0D/2D Mixed-Dimensional Heterostructure

Authors: Venkatarao Selamneni (Birla Institute of Technology and Science Pilani Hyderabad Campus, India); Chandra Sekhar Reddy Kolli (Birla Institute of Technology and Sciences Pilani Hyderabad campus, India); Parikshit Sahatiya (Birla Institute of Technology and Science Pilani Hyderabad Campus, India).

P-49: Transparent Photodetector Based on a Composite of Silver and Tungsten Oxide Nanowires

Authors: Meenu Maria Solly, Neha Sharma and Parasuraman Swaminathan (Indian Institute of Technology Madras, India)

P-50: Experimental Determination of Diffusivity of Backsheet and EVA for Silicon Photovoltaic Modules

Authors: Jigar Faria, Shikha Marwaha, Md Sadullah and Kunal Ghosh (Indian Institute of Technology Mandi, India)

P-51: In-Situ Grown Ag-TiO2 Based Plasmonic Hot-Electron Photo-Detector With Excellent Detectivity and Faster Response

Authors: Sobhan Hazra (Indian Institute of Technology (Banaras Hindu University), Varanasi, India); Satya Veer Singh (IIT BHU, India); Bhola Pal (IIT (BHU), Varanasi, India)

P-52: Synthesis of CuZnS Nanocrystals via Microwave Technique and Its' Application for Photodetector Device

Authors: Sandeep Dahiya (IITBHU, India); Satya Veer Singh (IIT BHU, India); Bhola Pal (IIT (BHU), Varanasi, India)

P-53: Charge Carrier Dynamics With Organic Hole Transport Layer on FASnI3 Perovskite

Authors: Basavaraju U (Indian Institute of Science & Central Manufacturing Technology Institute, India); Bidisha Nath, Sandeep Satyanarayana and Ashutosh P (Indian Institute of Science, India); Naga Hanumaiah (Central Manufacturing Technology Institute, India); Praveen C Ramamurthy (Indian Institute of Science, India)

P-54: Performance Optimization of Low-Cost Hybrid Perovskite Solar Cells Using Thickness Variation of Perovskite and Transport Layers

Authors: Deepak Kumar Jarwal (Pandit Deendayal Energy University, India); Rahul Kumar (Indian Institute of Technology Jodhpur, India); Santosh Kumar Satapathy (Pandit Deendayal Energy University, India & Assistant Professor, India); Amit Kumar (ABV-IIITM, India); Gopal Rawat (Indian Institute of Technology Mandi (IIT Mandi), India)

P-55: Self-Powered, Broadband (400-1800 Nm), Highly Responsive Photodetectors Based on Germanium Micropillars/Cu2ZnSnS4 Heterojunctions

Authors: Sudarshan Singh (Indian Institute of Technology Kharagpur, India); Arijit Sarkar (Gachon University South Korea, India); Ila Ashok (Indian Institute of Technology Kharagpur, India); Samit Kumar Ray (IIT Kaharagpur, India)

P-56: Effect of Ionic Liquids on 2D-3D Lead-Based Perovskite Solar Cells

Authors: Bhumika Sharma (Indian Institute of Science Bangalore Karnataka, India); Vani Pawar (Indian Institute of Sciences Bangalore, India); Satish Patil (Indian Institute of Science, India); Sushobhan Avasthi (Indian Institute of Science & Centre for Nano Science and Engineering (CeNSE), India)

P-57: Alpha Radiation Detection Using Si PIN Diodes

Authors: K Prabakar and O. k. Sheela (Scientist, India); Raghu Ramaiah M (Indira Gandhi Centre for Atomic Research, India); S Tripura Sundari (Scientist, India); Sandip Dhara (IGCAR, Kalpakkam, India)

P-58: Towards More Eco-Friendly Organic Solar Cells With PPDT2FBT: PCBM Active Layer Devices on Paper Substrates

Authors: Madhu Rawat (Indian Institute of Technology Kanpur, India); Arthur Hendsbee (Brilliant Matters, Canada); S. Sundar Kumar Iyer (Indian Institute of Technology Kanpur, India)

P-59: Combining Photo Electro Magnetic Effect and Photoconductivity to Measure Carrier Transport Properties in Semiconductors

Authors: Amritha A Raj (Indain Institute of Science, India); Shubhangi Bhardwaj (Indian Institute of Science Bangalore, India); Narasimhan K L (Indain Institute of Science, India); Sushobhan Avasthi (Indian Institute of Science & Centre for Nano Science and Engineering (CeNSE), India)

P-60: Effect of Spatial Trap Distribution Under Different Generation Profiles on J-V Characteristics of Bulk Heterojunction Organic Solar Cell

Authors: Harsh Kadole and S. Sundar Kumar Iyer (Indian Institute of Technology Kanpur, India)

P-61: High Efficiency Semitransparent Perovskite Solar Cells Tuned via Change in Concentration of Perovskite Precursor

Authors: Nisheka Anadkat (Indian Institute of Science, Bangalore, India); Shruti Shukla (Indian Institute of Science Bangalore, India); Sandeep Kumar (IISc Bangalore, India); Sushobhan Avasthi (Indian Institute of Science & Centre for Nano Science and Engineering (CeNSE), India)

P-62: Sputtered NiOx as a Hole Transport Layer in n-i-p Perovskite Solar Cells Manufactured on Steel Substrate

Authors: Sandeep Kumar (NTPC School of Business, India); Nisheka Anadkat (Indian Institute of Science, Bangalore, India); Mahek Mehta and Rich Kant (Indian Institute of Science Bangalore, India); Vani Pawar (Indian Institute of Sciences Bangalore, India); Sushobhan Avasthi (Indian Institute of Science & Centre for Nano Science and Engineering (CeNSE), India)

P-63: UV Treatment: A Simple and Convenient Way to Enhance the Performance of Organic Phototransistors

Authors: Sk Shahrukh (IIT Kharagpur, India)

P-64: Effect of Intrinsic Amorphous Layer Thickness and Annealing on the Performance of Silicon Heterojunction Solar Cells

Authors: Ashutosh Pandey, Shrestha Bhattacharya, Sourav Mandal and Jagannath Panigrahi (Indian Institute of Technology Delhi, India); Vamsi Komarala (IIT Delhi, India)

P-65: Analysis and Comparison of Full and Half-Cut Cell Monofacial and Bifacial PV Modules Under Realistic Shading Conditions

Authors: Nihaal S Adarsh (IIT Bombay & Undergrad at KJ Somaiya College of Engineering, India); Yogeswara Rao Golive and Narendra Shiradkar (Indian Institute of Technology Bombay, India)

Track: 2D Material Based Technologies (2DT)

P-66: Effect of Diverse Metal Contacts on Two-Dimensional Transition-Metal Dichalcogenides

Authors: Rahul Debnath (IISc Bangalore, India); Arindam Ghosh (India, India); Shaili Sett (UCL, India)

P-67: Wearable MoS2 Photodetector Based on Quasi-Dry Layer Transfer Process

Authors: Madan Sharma (Indian Institute of Technology Delhi, India)

P-68: High Performance CsPbI3 NCs Decorated Few-Layer WS2 Hybrid Photodetectors

Authors: Shreyasi Das (Indian Institute of Technology Kharagpur, India); Arup Ghorai (Pohang University of Science and Technology Korea, India); Sourabh Pal, Somnath Mahato, Soumen Das and Samit Kumar Ray (Indian Institute of Technology Kharagpur, India)

P-69: Impact of Process Induced Strain on the Sensitivity of Charge Plasma Doped TMD TFET Biosensor

Authors: Monika Kumari and Manodipan Sahoo (Indian Institute of Technology Dhanbad, India)

P-70: Modeling of Particle Growth in Thin Films

Authors: Rahul Basu (VTU & JNTU, India)

P-71: Vertically Stacked Atomic Layered MoS2-ReS2 Heterostructures by Chemical Vapor Deposition

Authors: Parikshit Sahatiya (Birla Institute of Technology and Science Pilani Hyderabad Campus, India); Chandra Sekhar Reddy Kolli (Birla Institute of Technology and Sciences Pilani Hyderabad campus, India); Gowtham Polumati (Birla Institute of Technology Science Pilani Hyderabad Campus, India)

P-72: Studies on the Avalanche Response Time-Delay Due to Photo-Illumination in <H-ATT> Device Design Optimized at Terahertz Regime

Authors: Debraj Chakraborty (Adamas University, India); Abhijit Kundu and Saunak Bhattacharya (Chaibasa Engineering College, India); Moumita Mukherjee (Adamas University, India)

P-73: Controlled Growth of Electronic Grade 2D MoSe2-WSe2 Lateral Heterostructure and Optoelectronic Characteristics

Authors: Purbasha Ray (Indian Institute of Technology, Kharagpur, India); Baisali Kundu and Biswajeet Nayak (Indian Institute of Technology Kharagpur, India); Monalisa Pradhan (Kalinga Institute of Industrial Technology Bhubaneswar, India); Suman Kumar Chakraborty, Rajdeep Banerjee, Soumen Giri and Rabaya Basori (Indian Institute of Technology Kharagpur, India); Gopal K Pradhan (Kalinga Institute of Industrial Technology Bhubaneswar, India); Dipak Kumar Goswami (IIT KHARAGPUR, India); Prasana Kumar Sahoo (Indian Institute of Technology Kharagpur, India)

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P-75: Investigation of Structural, Electronic and Transport Properties of Silicene on Graphene Heterostructure by Ab-Initio Calculations

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Authors: Ashraf Maniyar (IIT PATNA, India); P s t n Srinivas (Indian Institute of Technology Patna, India); P. Tiwari (IIT Patna, India)

P-80: Solution-Processed LiNbO3 Thin Film as a Gate Dielectric of a Ferroelectric Thin Film Transistor

Authors: Rajarshi Chakraborty (Indian Institute of Technology (Banaras Hindu University), Varanasi, India); Nila Pal (IIT BHU Varanasi, India); Bhola Pal (IIT (BHU), Varanasi, India)

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Authors: Anupama Anand (University of Delhi, India); Rakhi Narang (Sri Venkateswara College & University of Delhi, India); Dipendra Singh Rawal (Senior Scientist, India); Meena Mishra (Scientist F, India); Manoj Saxena (Deen Dayal Upadhyaya College & University of Delhi, India); Mridula Gupta (Semiconductor Device Research Laboratory, India)

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Authors: Aneesh M Joseph (Indian Institute of Technology, Bombay, India)

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Authors: Indrajit Das, Shashank Tiwari, K. T. Muhammed Shafi, Varuna Baipadi and Venkata Narayana Rao Vanukuru (Globalfoundries, India)

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P-123: AlGaN/GaN HEMTs on Silicon With a Graded-AlGaN Back-Barrier for RF Applications

Authors: Aniruddhan Gowrisankar, Vanjari Charan, Abheek Bardhan and Anirudh Venugopalarao (Indian Institute of Science, India); Hareesh Chandrasekar (AGNIT Semiconductors, India); Rangarajan Muralidharan (Indian Institute of Science, India); Srinivasan Raghavan (Indian Institute of Science & Centre for Nano Science and Engineering, India); Digbijoy Nath (Indian Institute of Science Bangalore India, India)

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